Emerging Challenges and Solutions For Signal Integrity and Jitter Testing For PCIe 2.0 @ 5 GT/s

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CTO

Wavecrest

Outline

I. High-speed I/O test review
- Link architecture evolution
- Jitter, noise, and signaling
- BER and interoperability

II. PCIe 2.0 jitter and signaling test requirements
- Link architecture overview
- Jitter, noise, and BER (JNB) transfer functions
- JNB and signaling tests (Tx, Rx, and Ref clock)

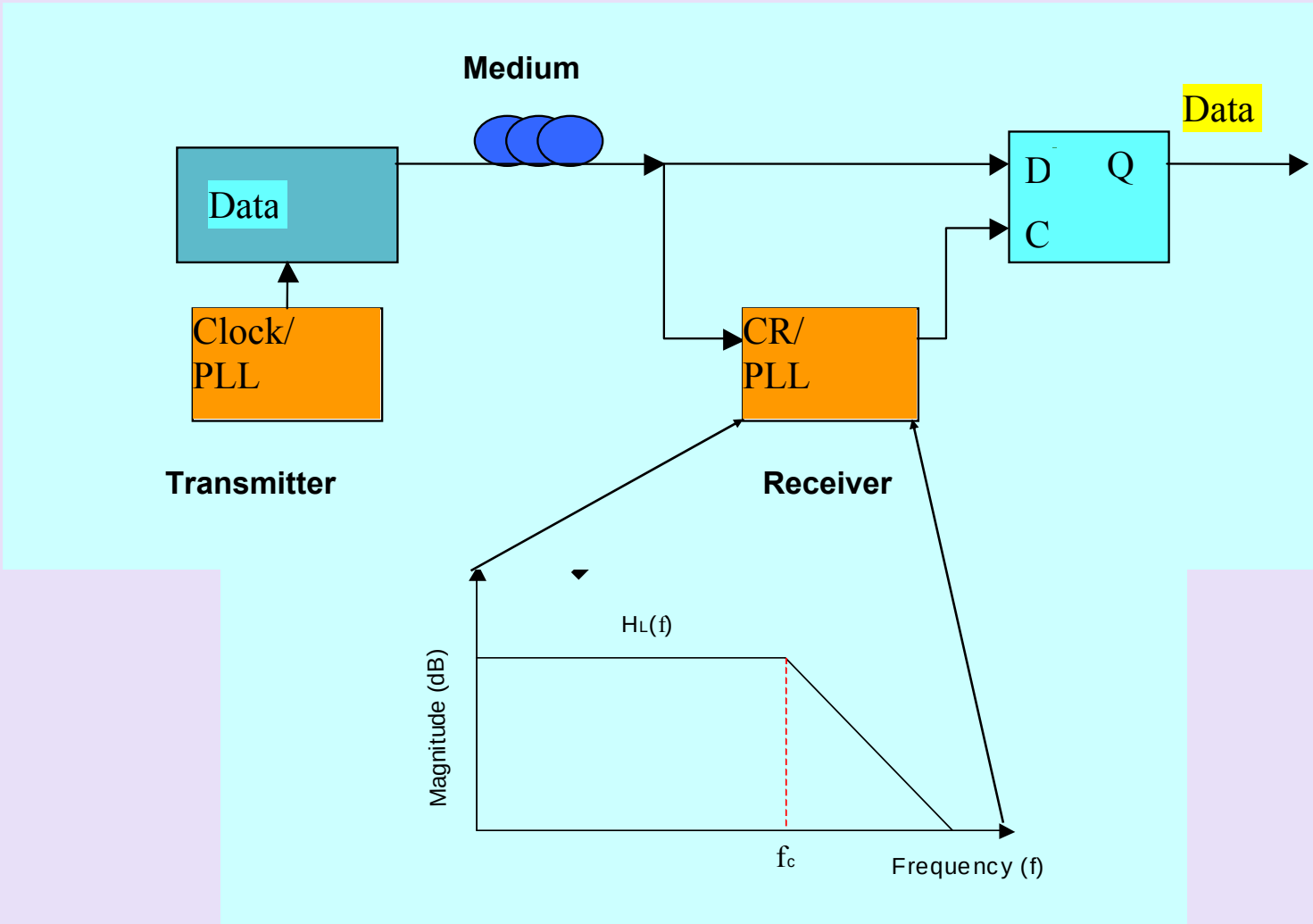
III. Test methods meeting requirements
- Transmitter
- Receiver
- PLL
- Ref clock

IV. Applications and case studies
- Compliance test
- Diagnostic test

V. Summary and conclusion

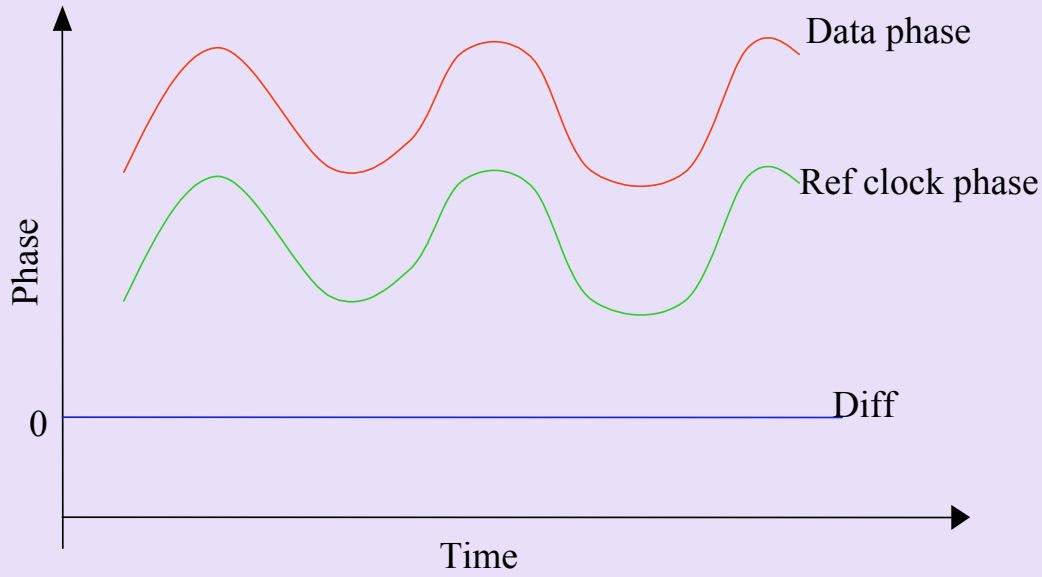
I: High Speed I/O Test Review

A Serial Data Communication System

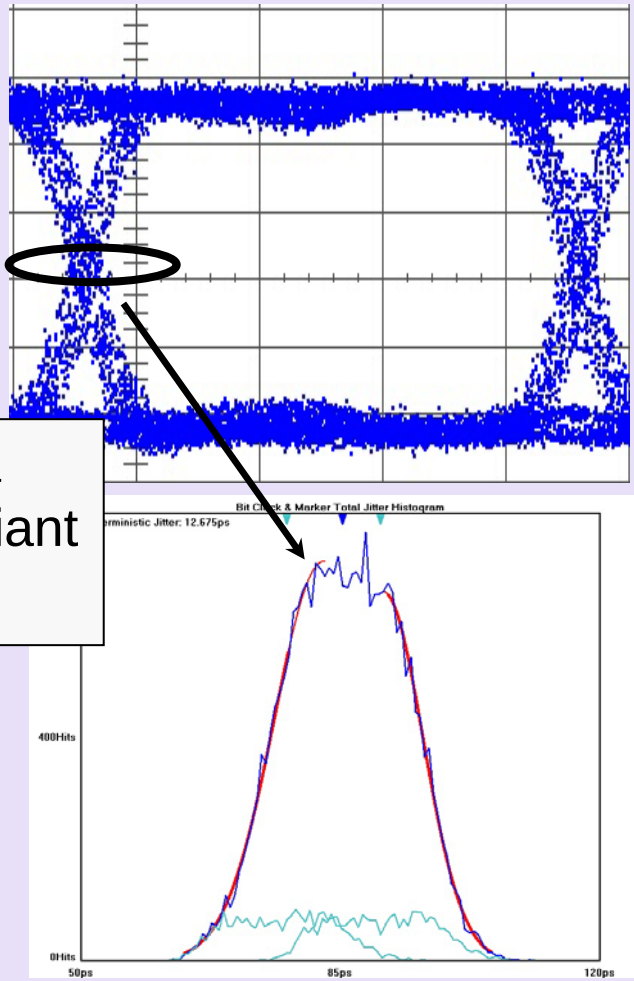


Phase Jitter Measurement and Reference Clock Used

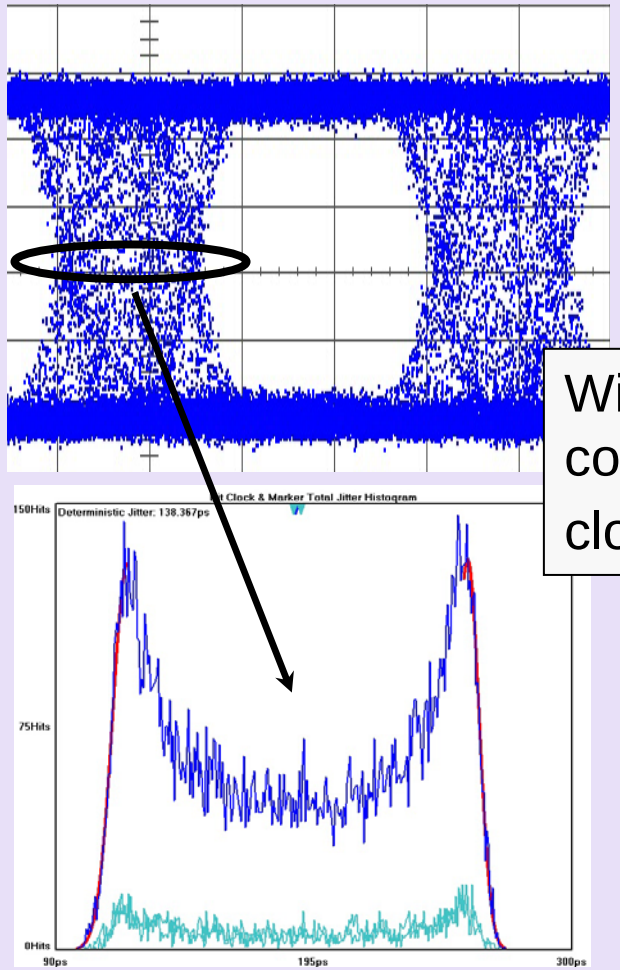
- Calculating Phase Jitter against a tracking clock (or recovered clock) reduces the amount of Phase Jitter calculated
- The amount of tracking depends on the recovered clock's transfer function of the receiver



Effect of Clock Recovery On Signal/Jitter Measurements



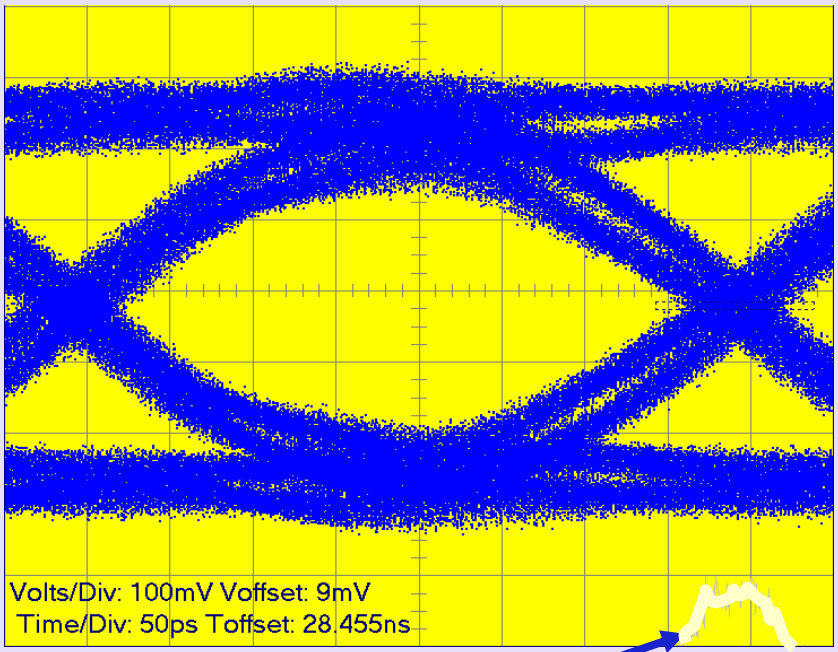
With a compliant clock

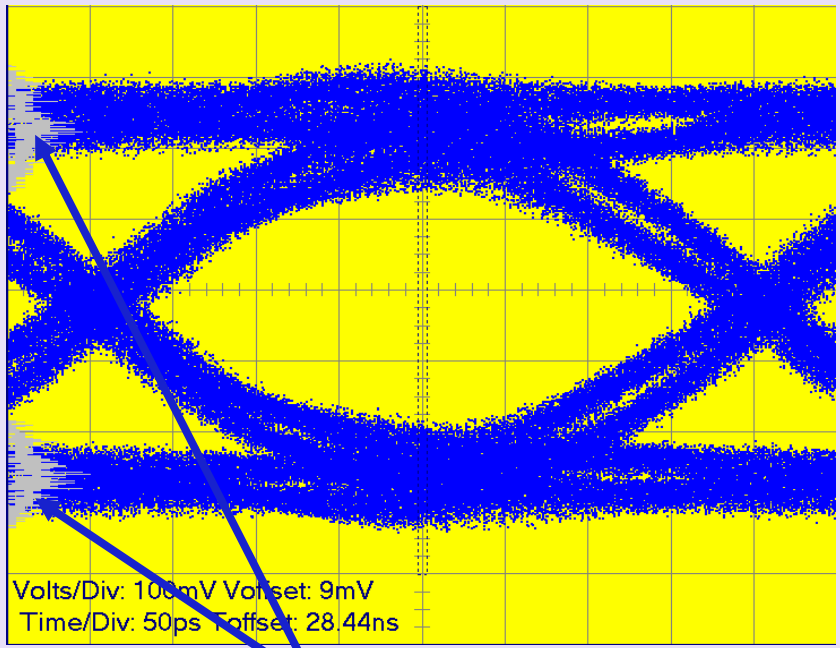


Without a compliant clock

Timing Jitter, Amplitude Noise, and BER (JNB)

- Timing jitter and amplitude noise can both cause bit errors to occur
- Bit Error Rate (BER) needs to be 10^{-12} or smaller
- Interoperability is merited by jitter, noise, and BER





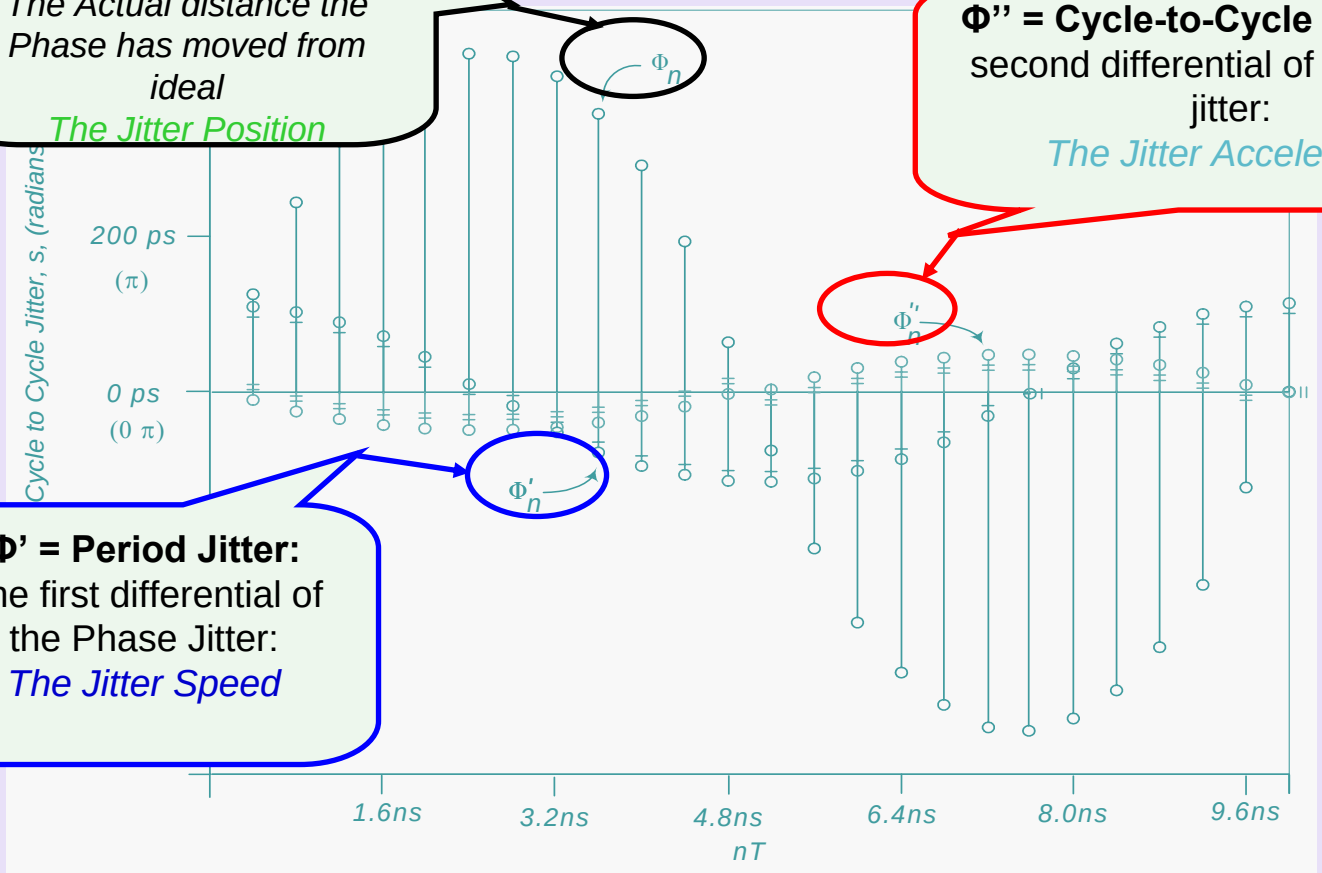
Timing jitter pdf

Amplitude noise pdf

Phase, Period, and Cycle-to-Cycle Jitter

Φ = Phase Jitter:
The Actual distance the Phase has moved from ideal
The Jitter Position

Φ'' = Cycle-to-Cycle Jitter: The second differential of the Phase jitter:
The Jitter Acceleration



Φ' = Period Jitter:
The first differential of the Phase Jitter:
The Jitter Speed

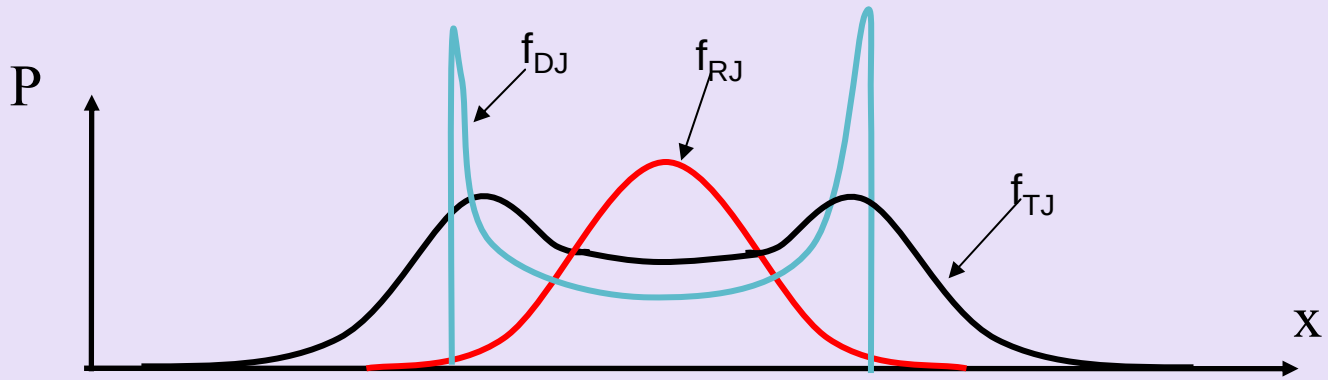
Law for PDFs: *Convolution*

- Convolution is defined by the following equation:

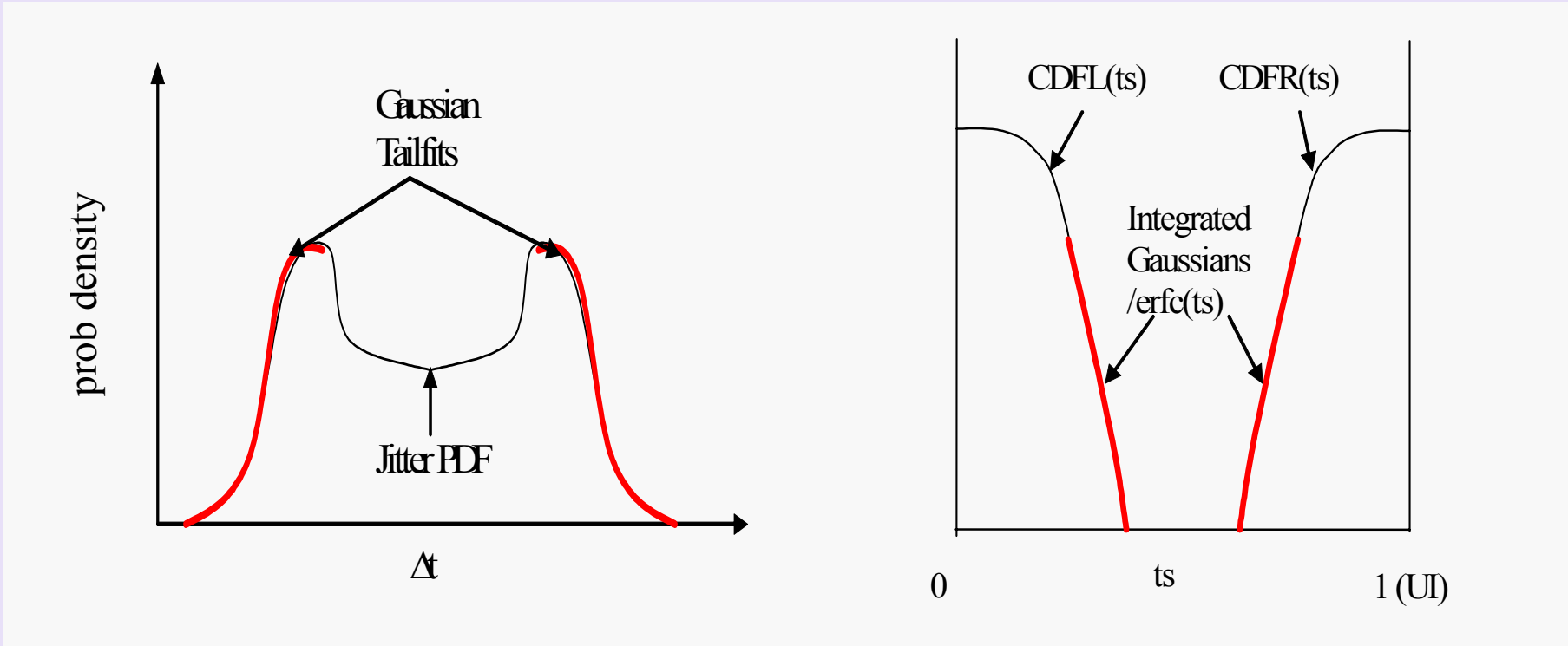
$$f(x) * g(x) = \int_{-\infty}^{+\infty} f(u)\, g(x-u)\, du$$

- The Total Jitter PDF is equal to the convolution of RJ PDF with the DJ PDF. This is shown in this equation:

$$f_{TJ}(x) = f_{RJ}(x) * f_{DJ}(x) = \int_{-\infty}^{\infty} f_{RJ}(u) \cdot f_{DJ}(x-u)\, du$$



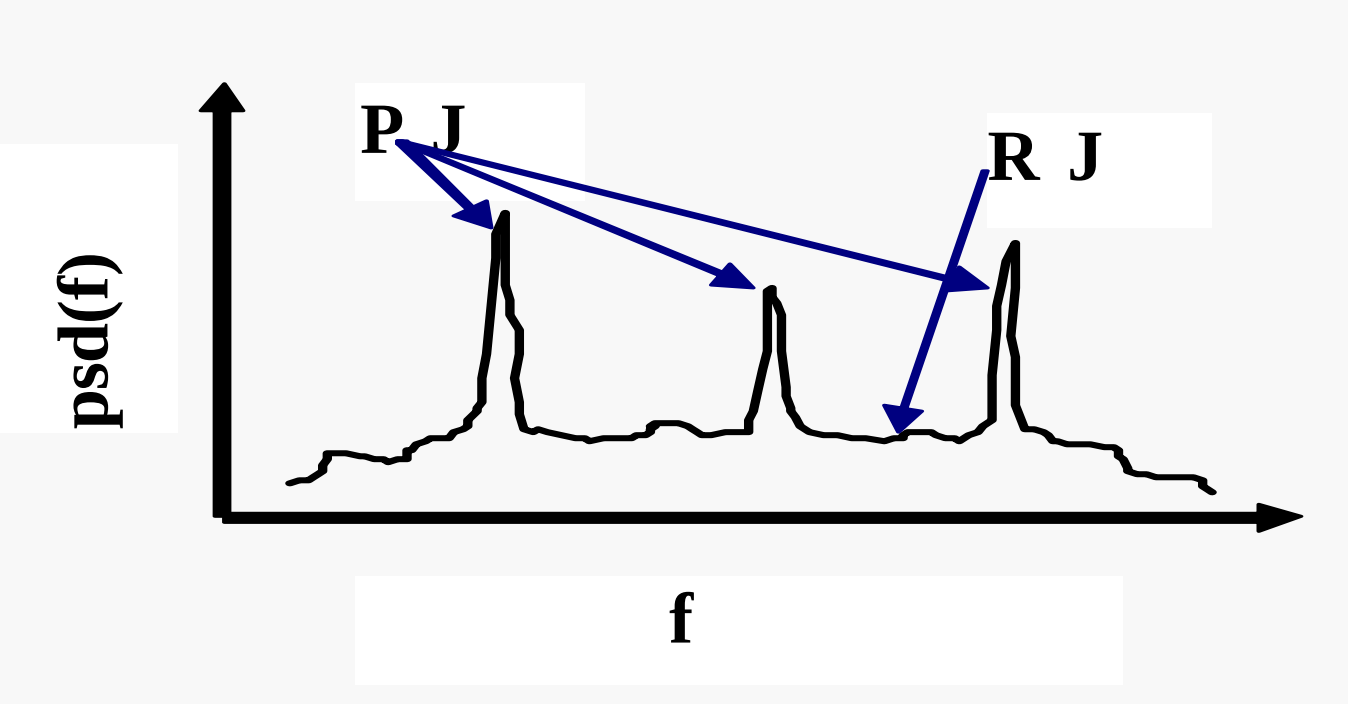
Jitter Separation (I): PDF or BER CDF Domain with TailFits



(a)

(b)

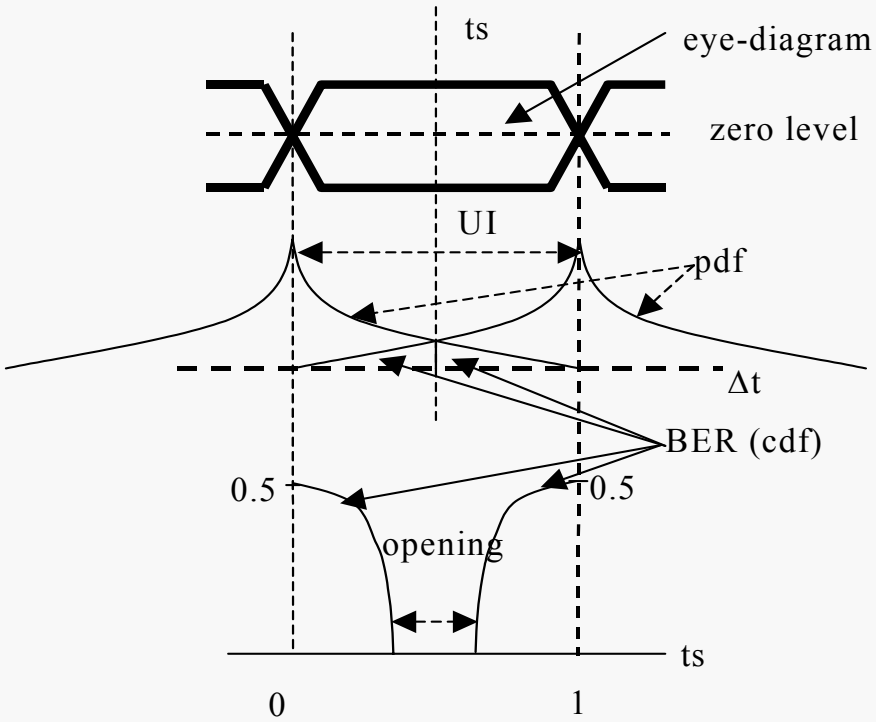
Jitter Separation (II): Time or Frequency Domain with Autocorrelation or PSD



- RJ PSD
- PJ PSD
- DDJ (DJ without PJ and BUJ) PSD

Jitter PDF, BER CDF, and Eye-Diagram

- Relationship of Eye Diagram, TJ PDF and BER CDF

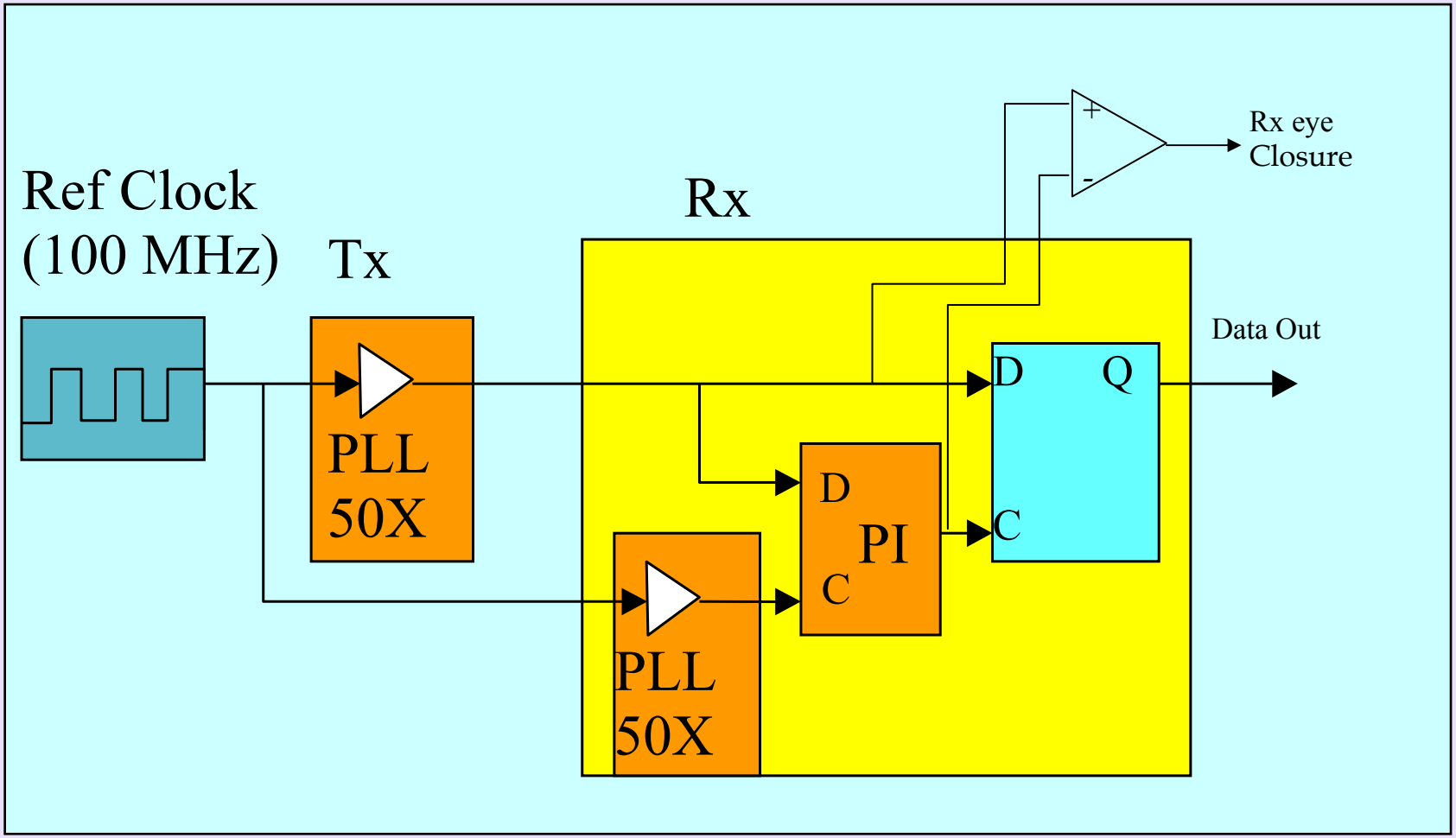


$$BER(t_s) = \frac{1}{2}\left[\int_{t_s}^{\infty} f_{TOT}(t)dt + \int_{-\infty}^{t_s} f_{TOT}(t - UI)dt\right]$$

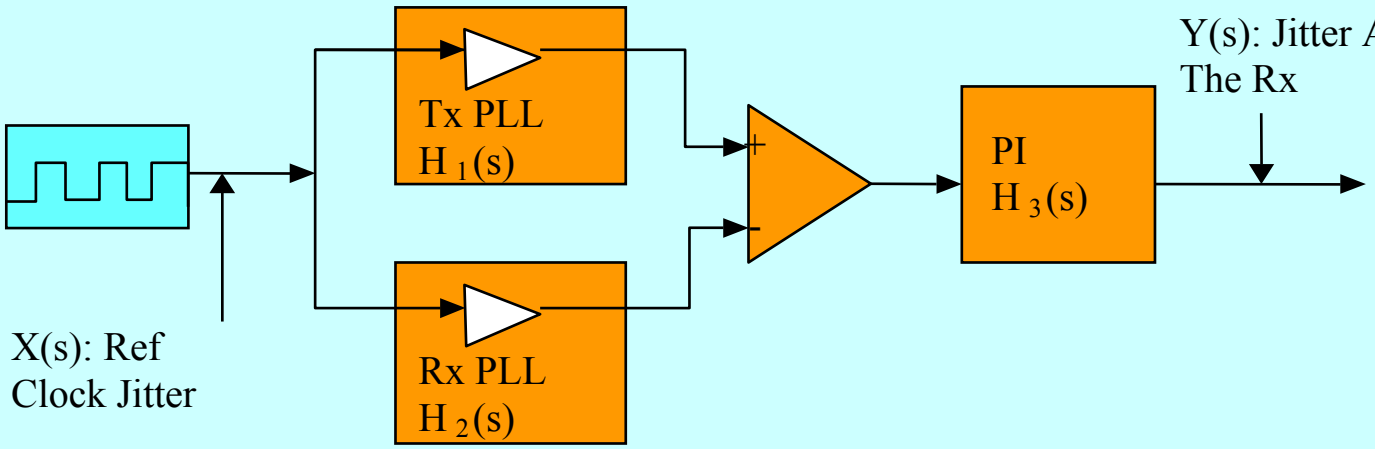
II: PCIe 2.0 Test Requirements

IMPORTANT NOTE: Numbers highlighted in green are from the 0.7 Draft of the PCIe 2.0 Specification and are *subject to change* before the final specification! They are presented for illustrative purposes only.

PCIe 2.0 Link Architecture (PI or OS Based)



System Transfer Functions

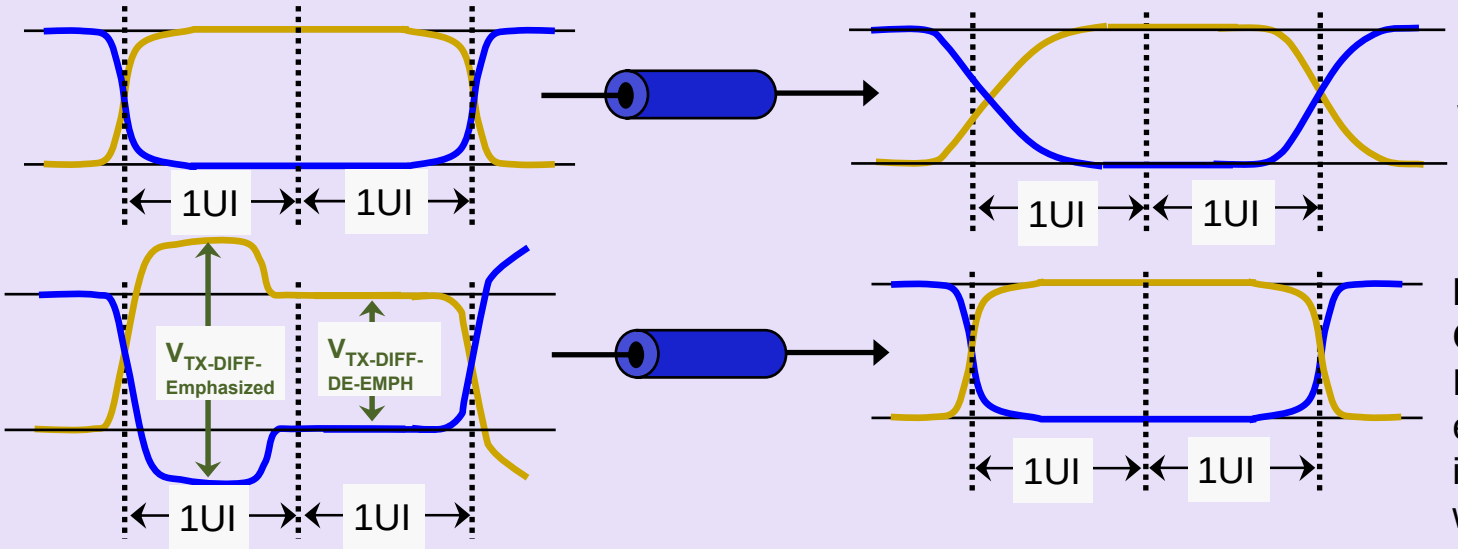


$$Y(s) = H_t(s)X(s) = \{[H_1(s)e^{-sT_d} - H_2(s)]H_3(s)\}X(s)$$

Tx Amplitude Voltage Test Requirements

Symbol	Parameter and Definition	2.5 GT/s (PCIe 1.x)	5 GT/s – PCIe 2.0 Draft 0.7	Unit
VTX-DIFF-PP	Differential p-p Tx voltage swing	0.8 (min) 1.2 (max)	**0.8 (min)** **1.2 (max)**	V
VTX-DE-RATIO -	Tx de-emphasis level	3.0 (min) -4.0 (max)	**-5.5 (min)** **-6.5 (max)**	dB

De-Emphasis



Channel Slows Edges: Bit window is reduced: Data Dependent Jitter (DDJ)

De-Emphasis Compensates: Exaggerated edges at TX result in better Bit window at RX

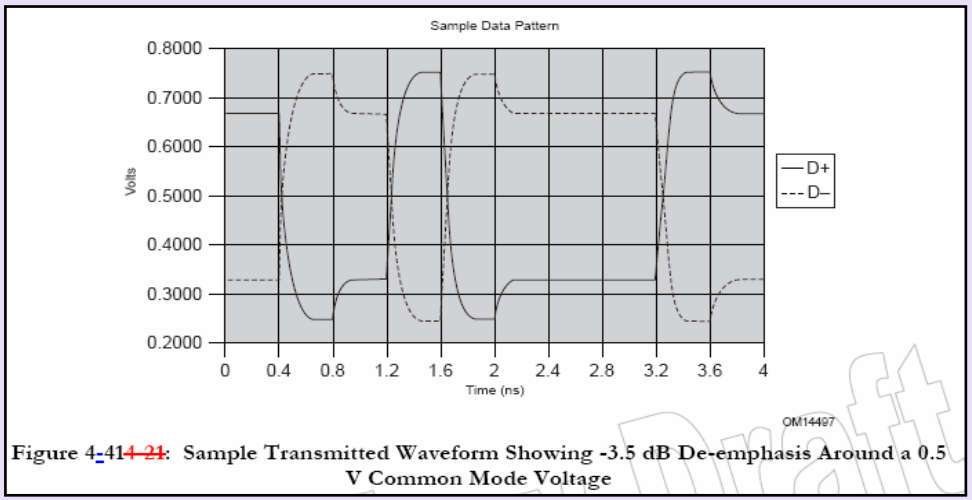
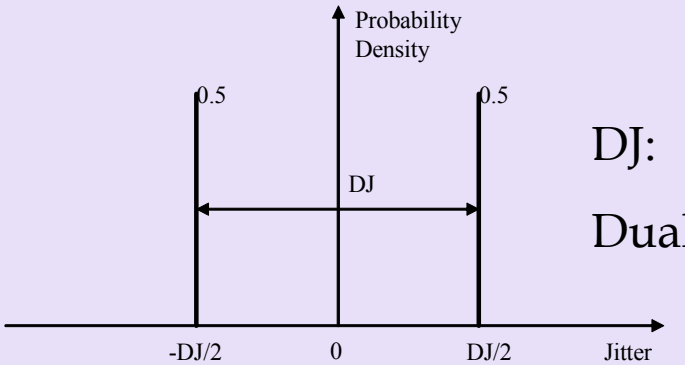


Figure 4-41~~4-21~~: Sample Transmitted Waveform Showing -3.5 dB De-emphasis Around a 0.5 V Common Mode Voltage

De-Emphasis tries to compensate for DDJ of the Channel

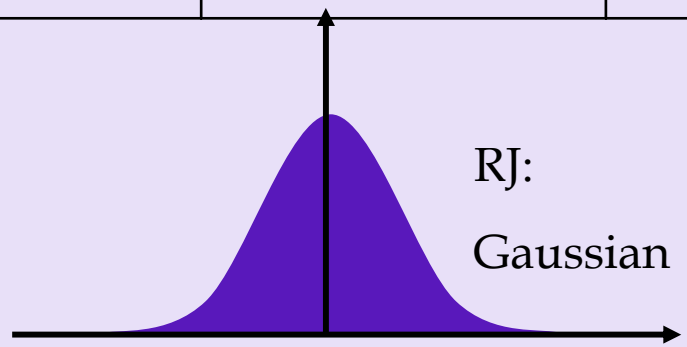
Tx Jitter/Timing Test Requirements

Symbol	Parameter and Definition	2.5 GT/s (PCIe 1.x)	5 GT/s (PCIe 2.0 Draft 0.7)	Unit
TMIN-PULSE	Instantaneous pulse width	Not spec'ed	**0.9 (min)**	UI
TTX-EYE	Transmitter Eye opening (@10^{-12} BER) including all jitter sources	0.75 (min)	**0.75 (min)**	UI
TTX-DJ-DD (max)	Tx deterministic jitter (DJ)	Not spec'ed	**0.15 (max)**	UI



DJ:

Dual-Dirac



RJ:

Gaussian

Tx PLL Test Requirements

Symbol	Parameter and Definition	2.5 GT/s (PCIe 1.x)	5 GT/s (PCIe 2.0 Draft 0.7)	Unit
BWTX-PLL	Maximum Tx PLL Bandwidth (BW)	22 (max)	**16 (max)**	MHz
BWTX-PLL-LO-3DB	Minimum Tx PLL BW for 3 dB peaking	3 (min)	**8 (min) MHz**	MHz
BWTX-PLL-LO-1DB	Minimum Tx PLL BW for 1 dB peaking	Not spec'ed	**5 (min)**	MHz
PKGTX-PLL1	Tx PLL peaking with 8 MHz min BW	Not spec'ed	**3.0 (max)**	dB
PKGTX-PLL2	Tx PLL peaking with 5 MHz min BW	Not spec'ed	**1.0 (max)**	dB

Tx Test Jitter Transfer Function

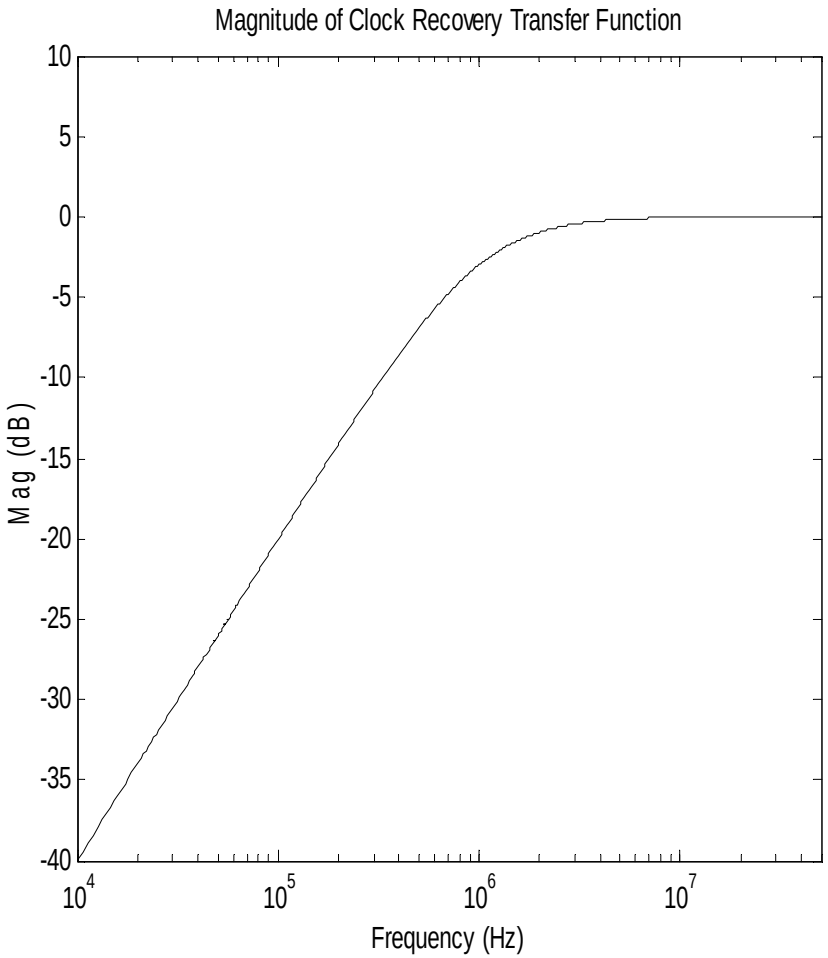
- 1st -order HPF of

$$H_3(s) = \frac{s}{s + \omega_3}$$

$$\omega_3 = 2\pi f_3$$

where

$$f_3 = 1.0MHz$$



Reference Clock Test Requirements

Symbol	Parameter and Definition	Min	Max	Unit
TPERIOD-ABS	Averaged instantaneous period (including SSC)	9.997	10.053	ns
VIH VIL	Differential Input High Voltage Differential Input Low Voltage	+150	-150	mV
VRB	Ring-back Voltage Margin	-100	+100	mV
$(dV/dt)_R$	Rising Edge Rate	0.6	4.0	V/ns
$(dV/dt)_F$	Falling Edge Rate	0.6	4.0	V/ns
η_{DC}	Duty Cycle	40	60	%
TCLK_RJ	**Ref clk RMS jitter**		**3.1**	**ps**
TSSC-JITTER-CC	SSC induced jitter that a receiver must track. Relevant only for common clock architecture		**65 ps PP at 33 KHz**	**ps**
TSSC-JITTER-DDC	SSC induced jitter that a receiver must track. Relevant only for data driving PLL architecture		**20 ns PP at 33 KHz**	**ns**

Reference Clock Jitter Transfer Function

$$H(s) = \left[H_1(s) * e^{-s * t\_delay} - H_2(s) \right]$$

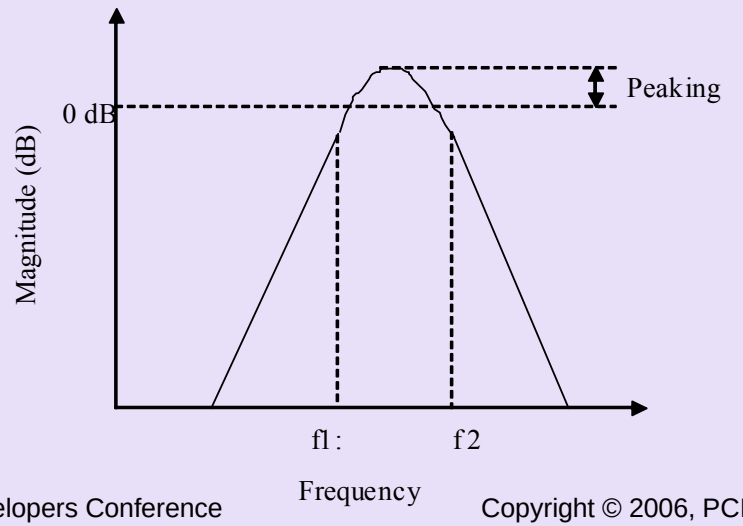
$$H_1(s) = \frac{2s\zeta\omega_1 + \omega_1^2}{s^2 + 2s\zeta\omega_1 + \omega_1^2}$$

$$H_2(s) = \frac{2s\zeta\omega_2 + \omega_2^2}{s^2 + 2s\zeta\omega_2 + \omega_2^2}$$

$$\zeta = 0.54$$

$$\omega_1 = \frac{2*\pi*8.61*10^6}{\sqrt{1+2\zeta^2+\sqrt{\left(1+2\zeta^2\right)^2+1}}} Rad/s$$

$$\omega_2 = \frac{2*\pi*4.31*10^6}{\sqrt{1+2\zeta^2+\sqrt{\left(1+2\zeta^2\right)^2+1}}} Rad/s$$



$$t\_delay = 12 \cdot 10^{-9} s$$

Rx Amplitude Voltage Test Requirements

Symbol	Parameter and Definition	2.5 GT/s (PCIe 1.x)	5 GT/s (PCIe 2.0 Draft 0.7)	Unit
VRX-DIFF-PP	Differential p-p Rx voltage swing	0.175 (min) 1.2 (max	**0.120 (min)** **1.2 (max)**	V
VRX-MAX-MIN-RATIO	Max to Min pulse voltage on consecutive UI	Not spec'ed	**5 (max)**	

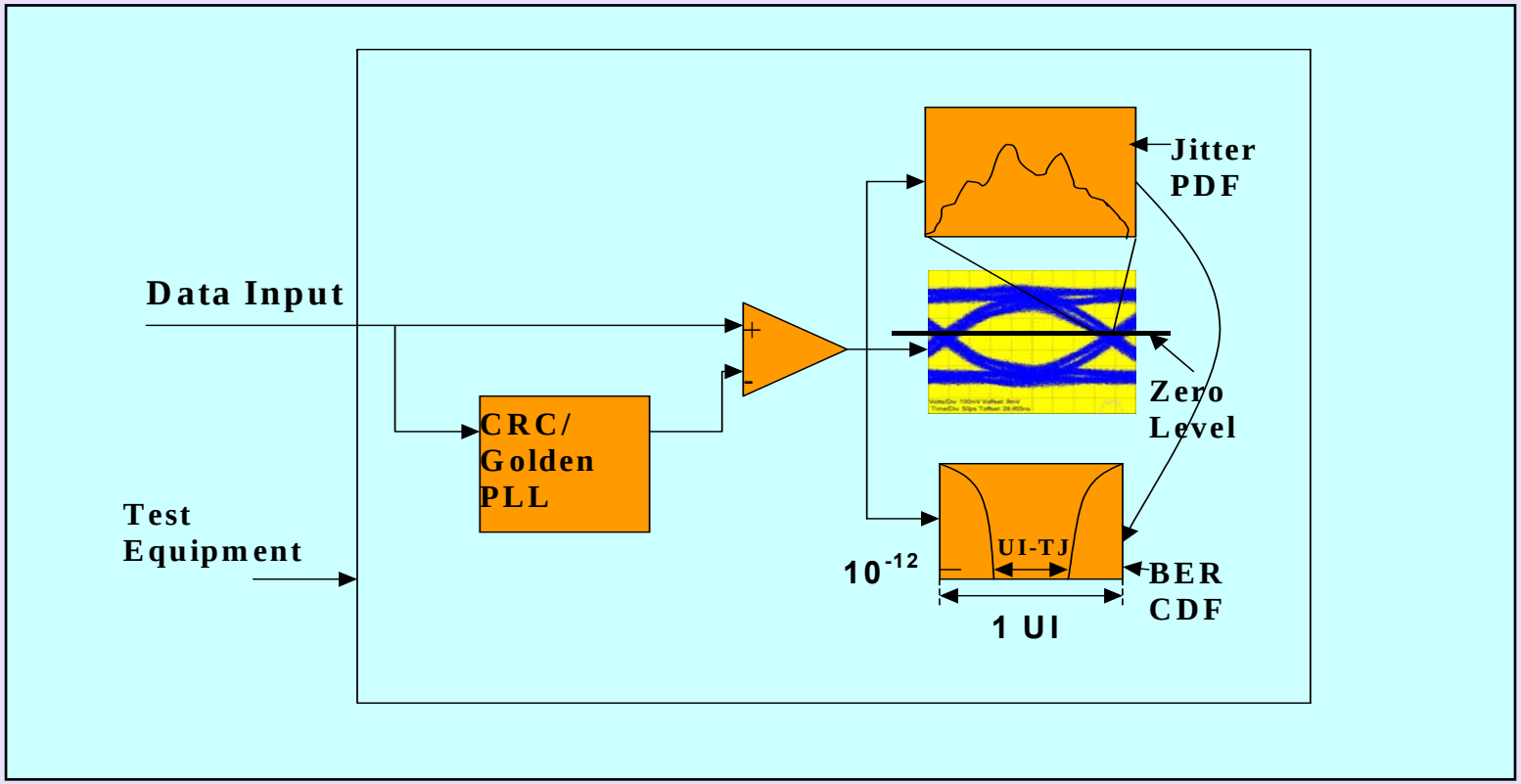
Rx Jitter/Timing Test Requirements

Symbol	Parameter and Definition	2.5 GT/s (PCIe 1.x)	5 GT/s (PCIe 2.0 Draft 0.7)	Unit
TRX-EYE	Receiver Eye opening (@10^{-12} BER)	0.4 (min)	**0.4 (min)**	UI
TRX-DJ-DD (max)	Rx deterministic jitter (DJ)	Not spec'ed	**0.44 (max)**	UI

III: Example Test Methods Meeting Requirements

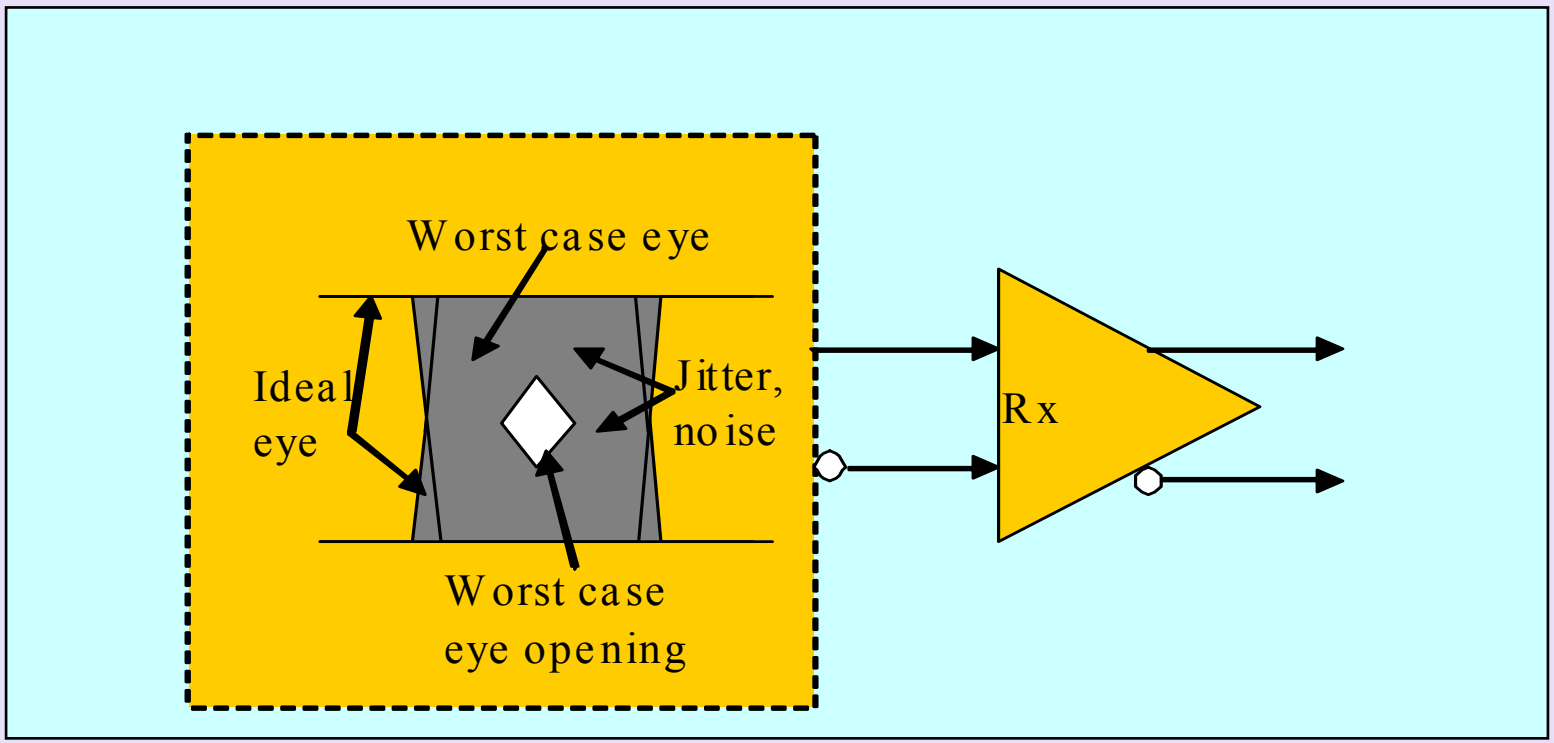
Example Tx Jitter/Signaling Test Methods

- Measure clock-to-data jitter
- TJ is measured at BER = 10^{-12}

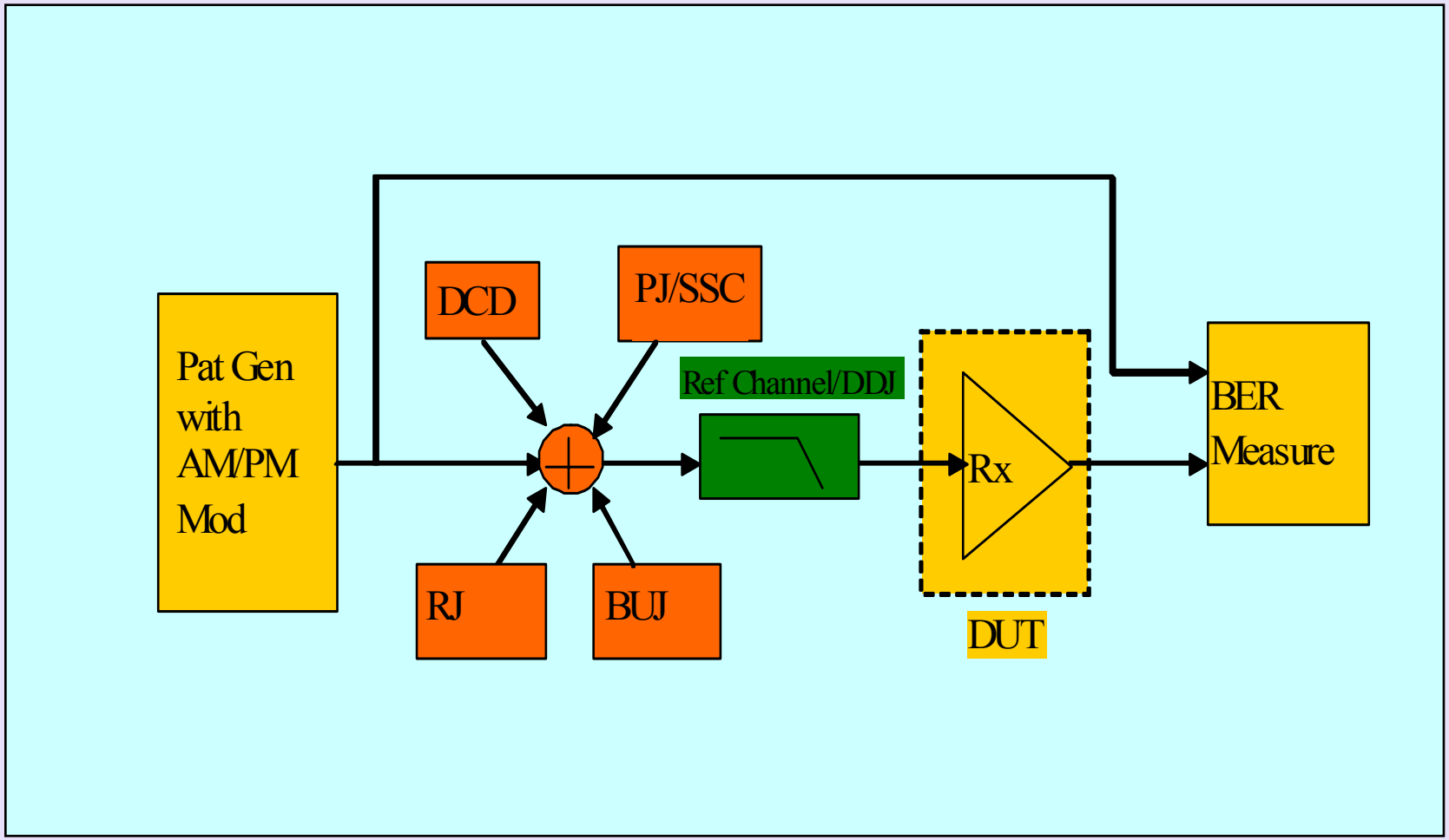


Example Rx Jitter/Signaling Test Methods

- Create the worst jitter/signaling conditions to stress the Rx and insure that it still meets the 10^{-12} BER requirement

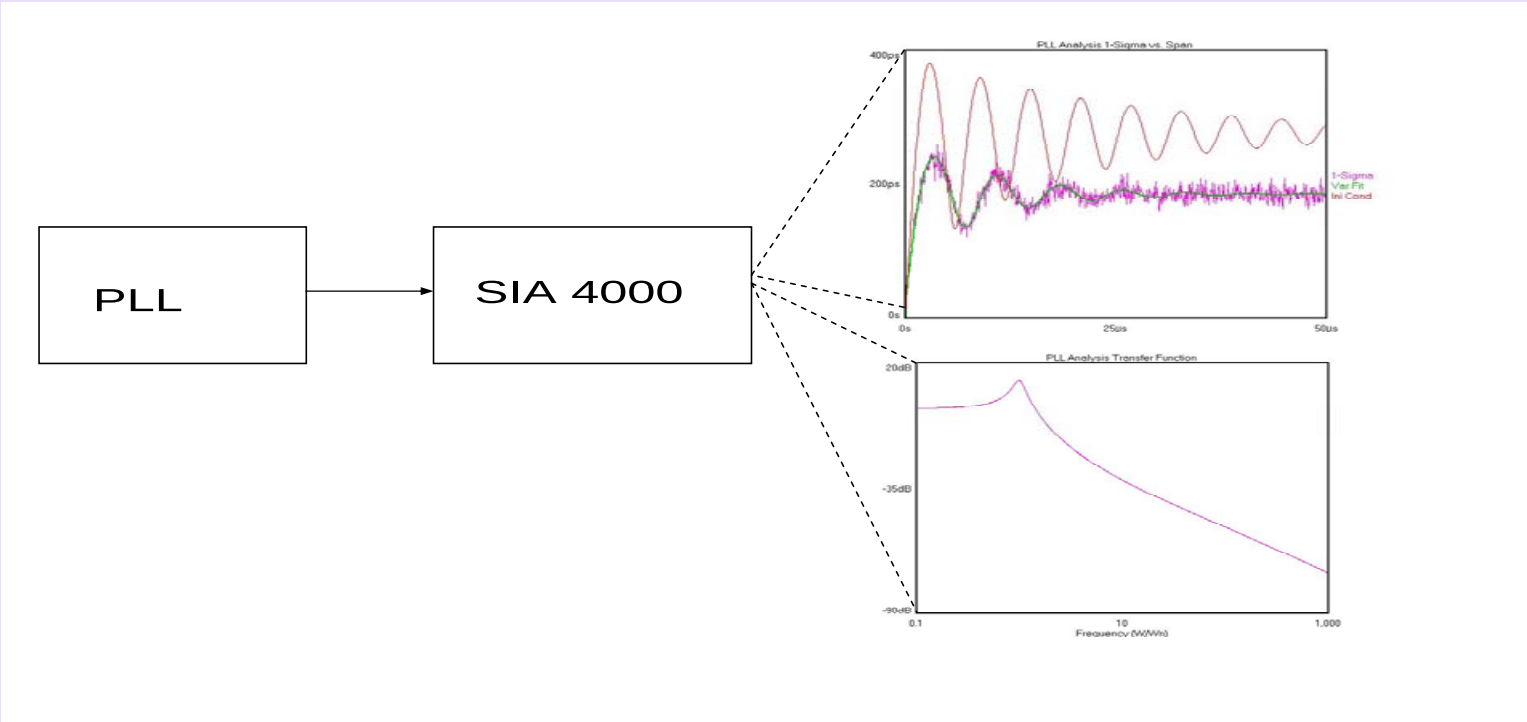


Example Rx Jitter/Signaling Test Method Cont…



Example PLL Test Methods

- One method will measure the PLL jitter variance function to derive the PLL transfer function (***No need*** for a stimulus, ***in-situ*** measurement)

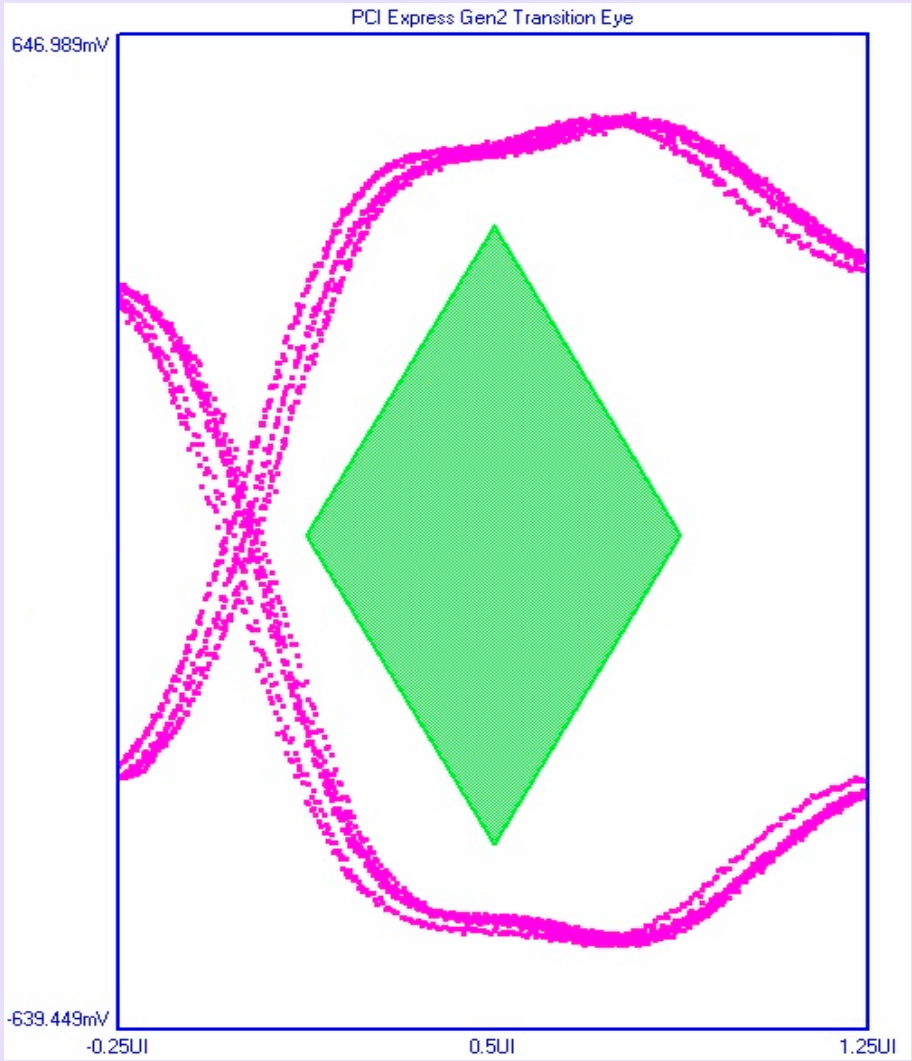


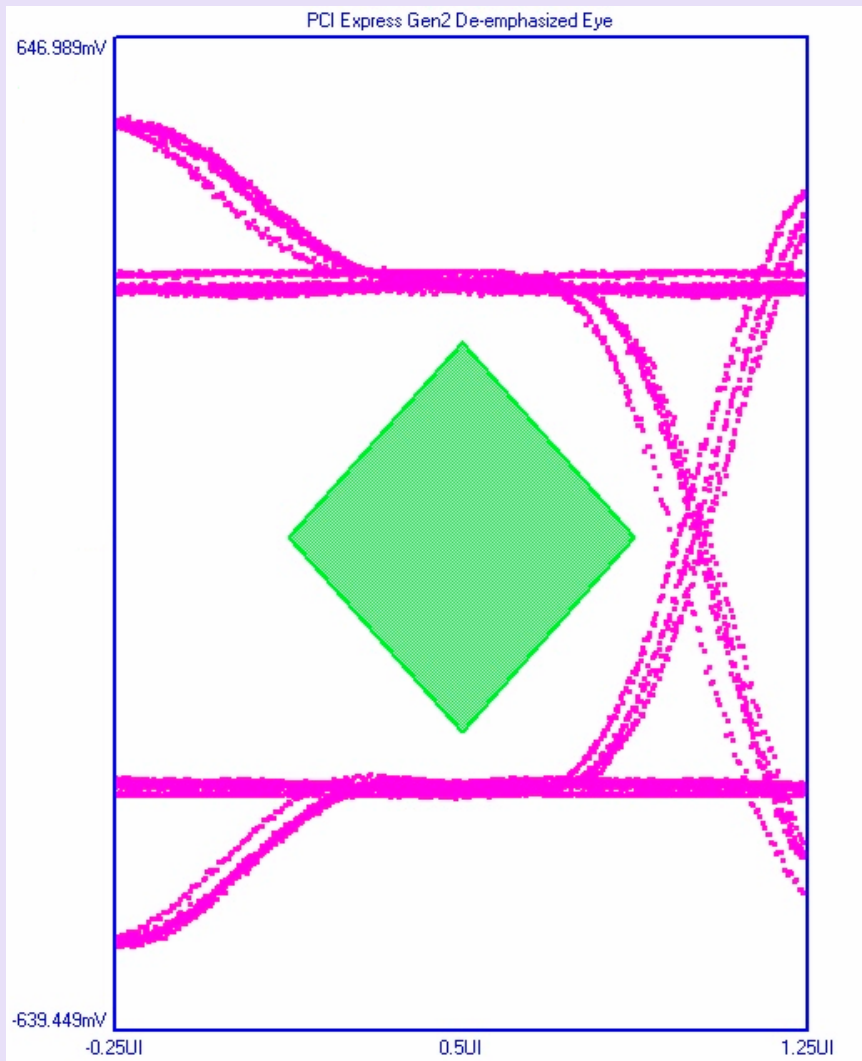
Example Reference Clock Jitter Test Methods

- Step 1: Measure the phase jitter time record, or spectrum, or power spectrum density (PSD)
- Step 2: Apply the required filter function in either time-domain, or frequency-domain
- Step 3: Estimate the RMS value after the filter function.

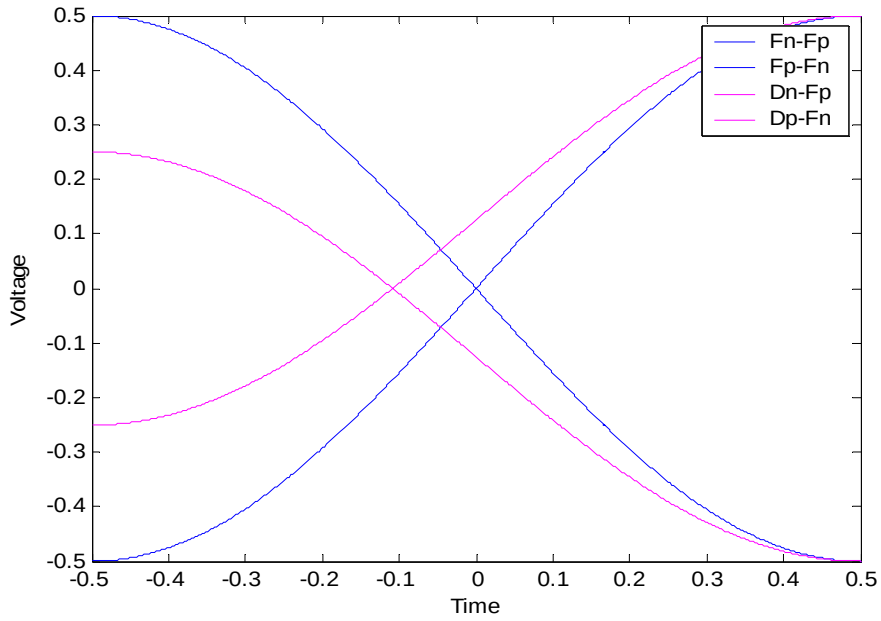
IV: Application and Case Study Examples

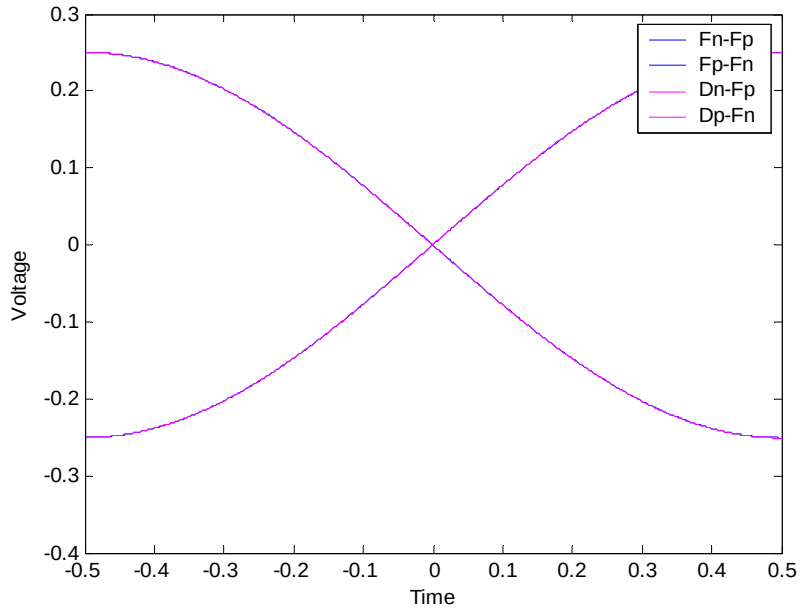
Tx Testing (I): Full Swing and De-Emphasis Eye



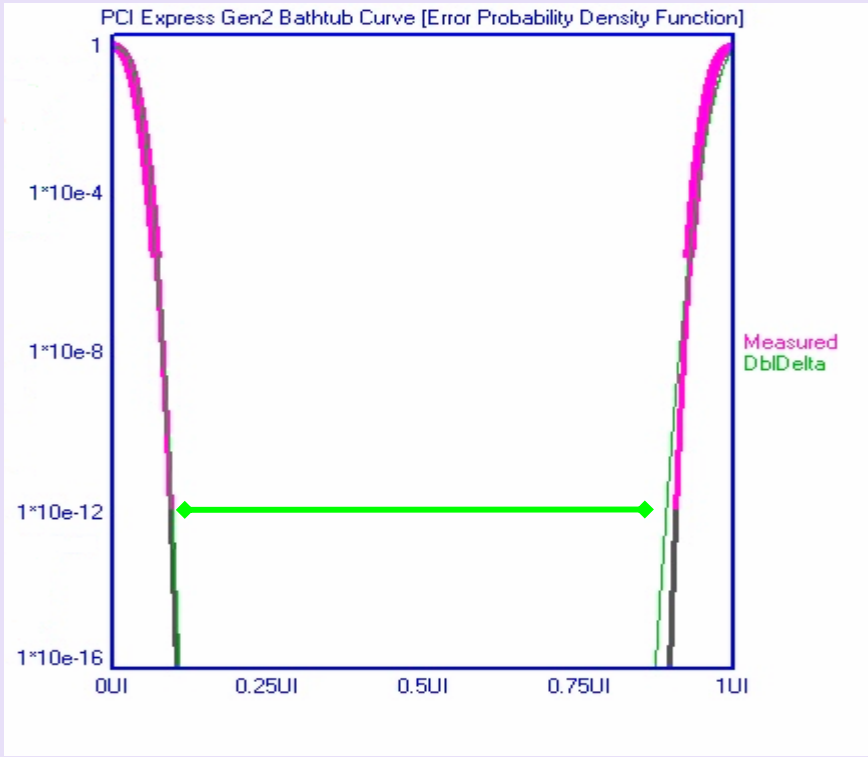


Tx Testing (II): De-Emphasis Induced Jitter Removal



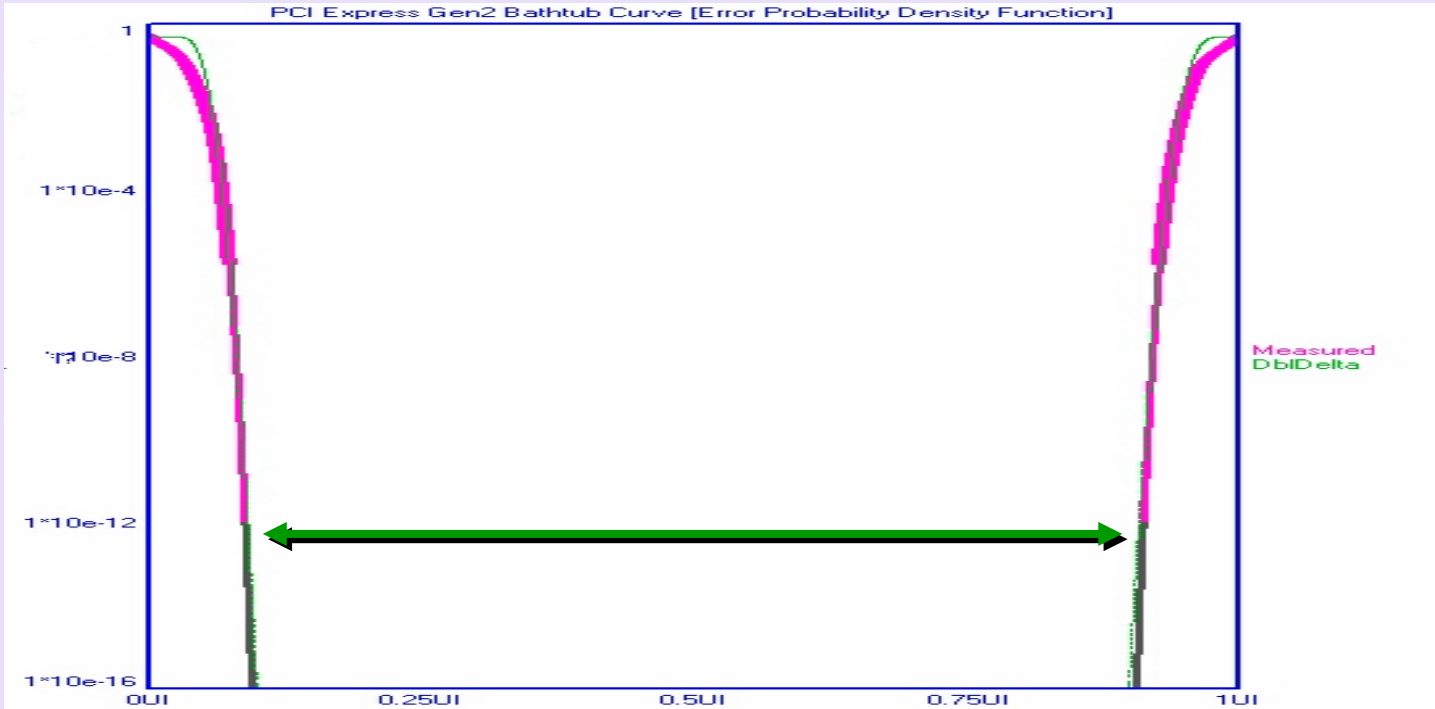


Tx Testing: DJ and TJ



TIMING MEASUREMENTS			
Quantity	**Specification**	**Measured**	**Pass/Fail?**
UI	**199.94ps-200.06ps**	**200ps**	**PASS**
TtxEye 10e-12	**>0.75UI**	**0.813816UI**	**PASS**
TtxDjDD	**<0.15UI**	**0.031209UI**	**PASS**
TtxRj		**0.011070UI**	

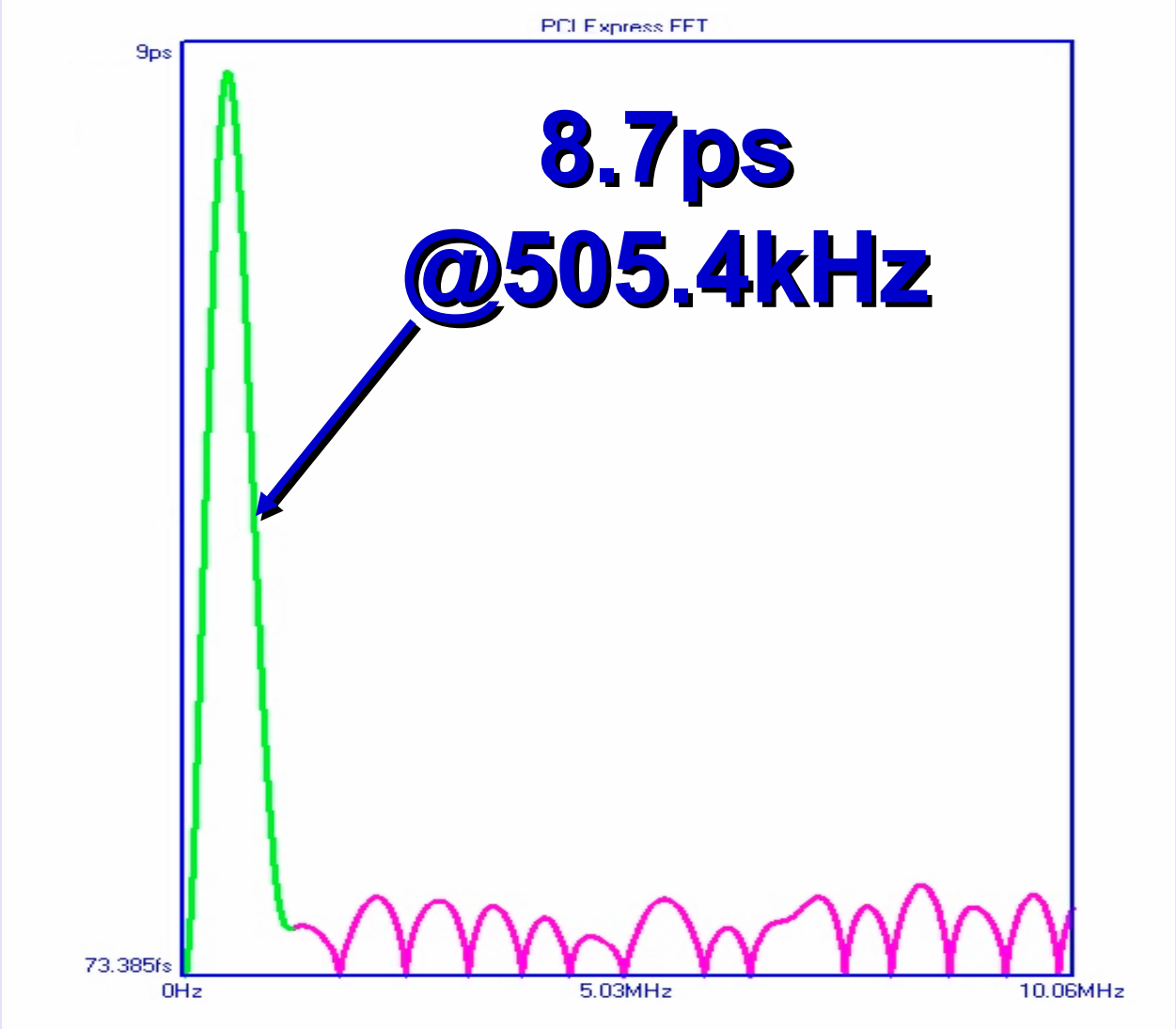
Tx Testing (II): DJ and TJ, Passing



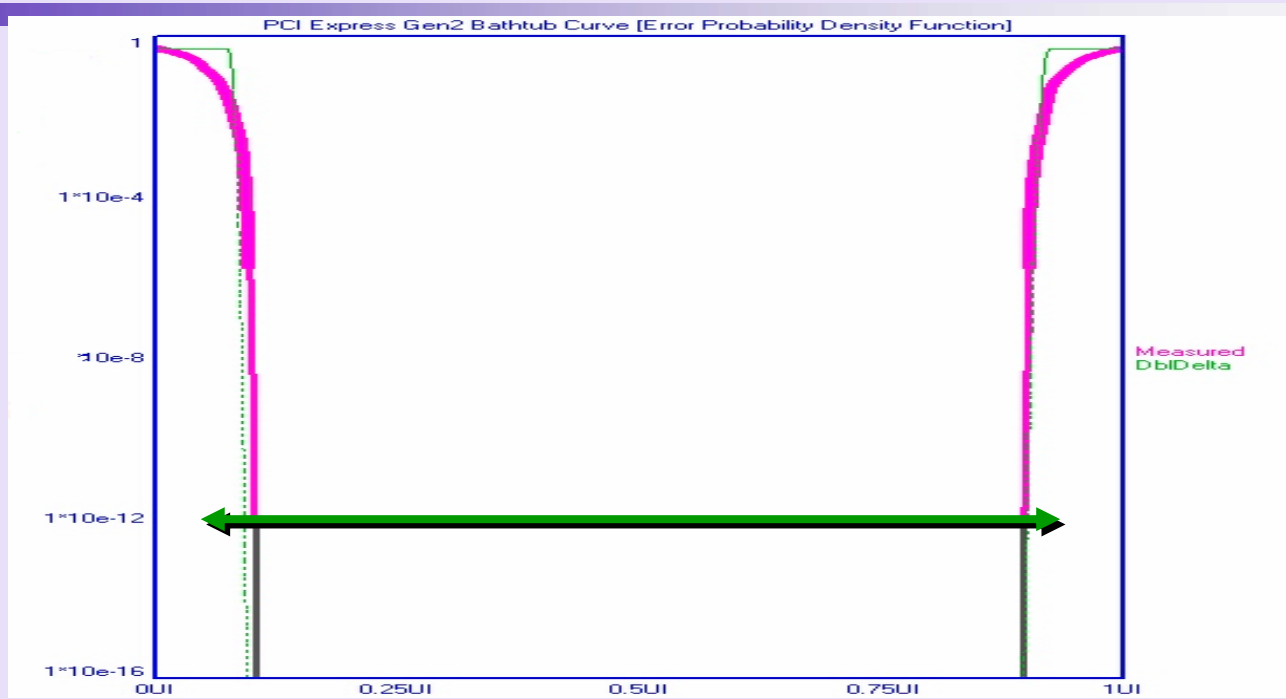
TIMING MEASUREMENTS

Quantity	Specification	Measured	Pass/Fail?
UI	199.94ps-200.06ps	200ps	PASS
TtxEye 10e-12	>0.75UI	0.824608UI	PASS
TtxDjDD	<0.15UI	0.076184UI	PASS
TtxRj		0.007086UI	

Tx Testing (II): PSD



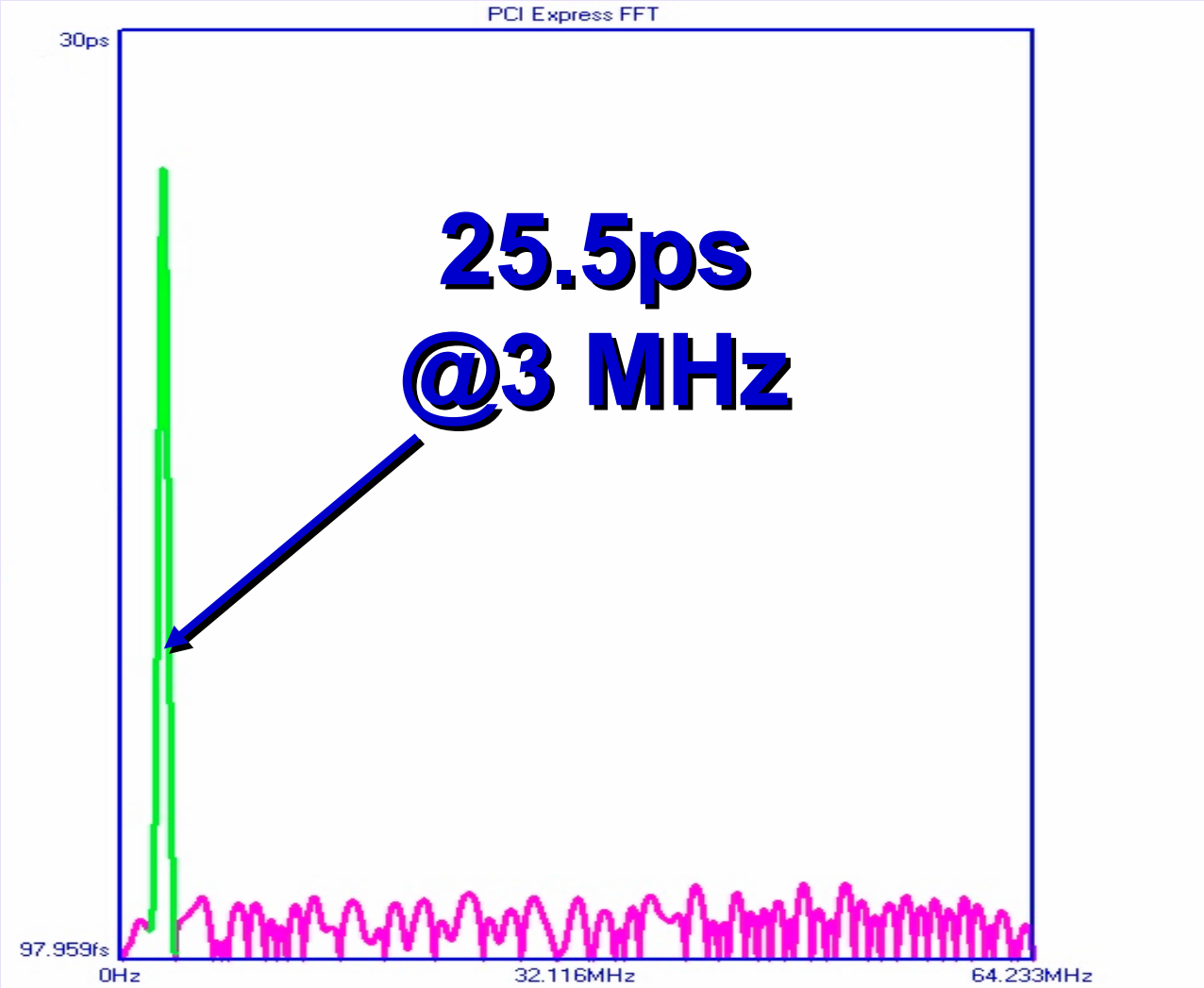
Tx Testing (III) DJ and TJ, Failing



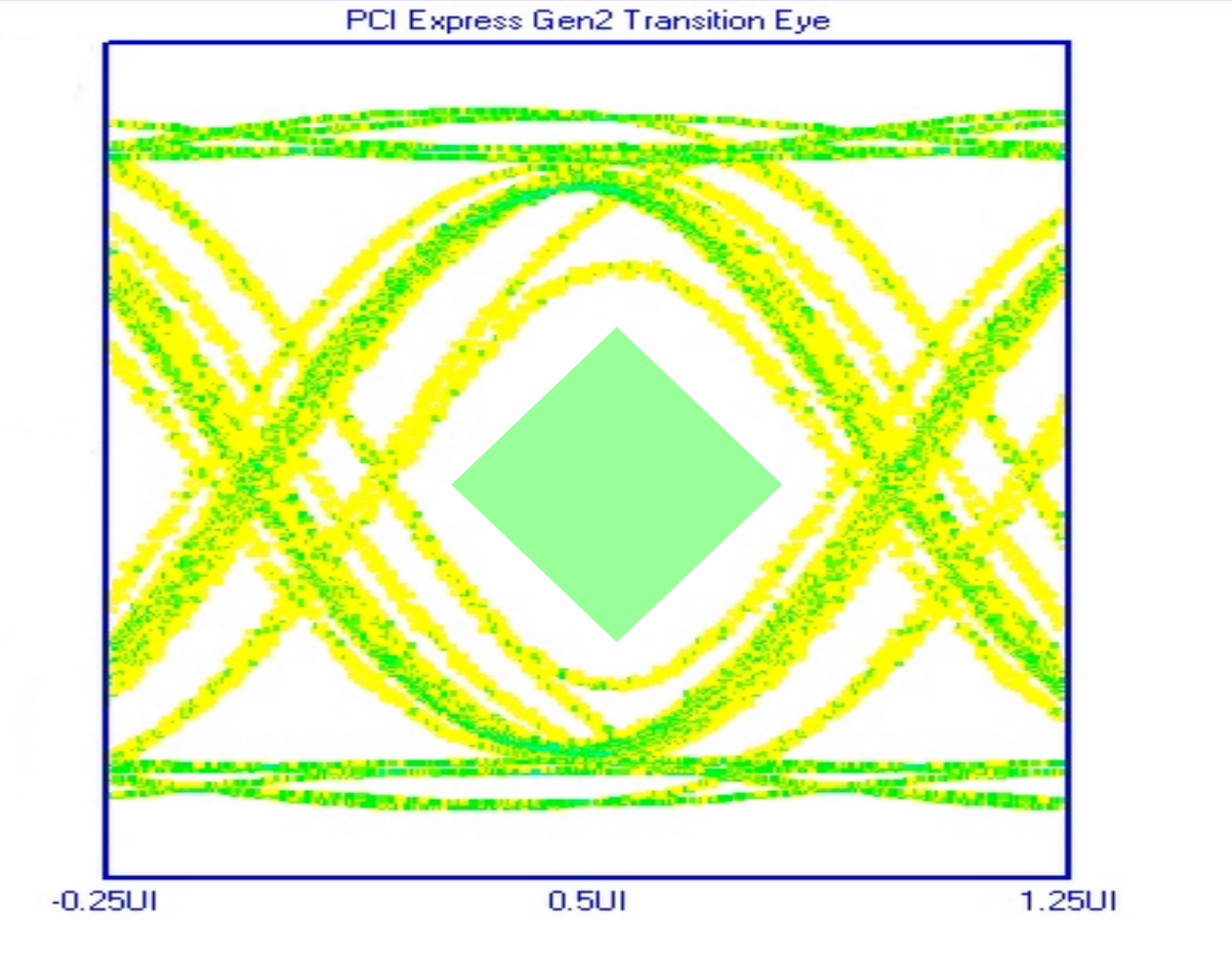
TIMING MEASUREMENTS

Quantity	Specification	Measured	Pass/Fail?
UI	199.94ps-200.06ps	200ps	PASS
TtxEye 10e-12	>0.75UI	0.744601UI	FAIL
TtxDjDD	<0.15UI	0.160213UI	FAIL
TtxRj		0.006799UI	

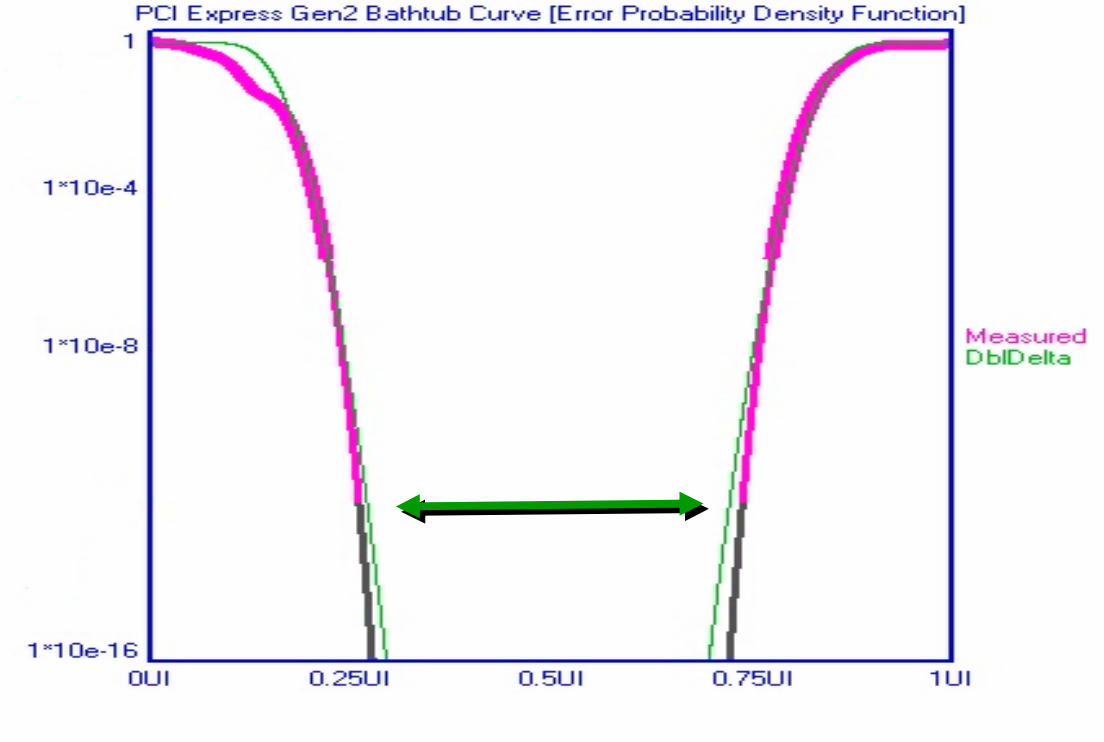
Tx Testing (III): PSD



Rx Testing: Compliance Eye-Diagram



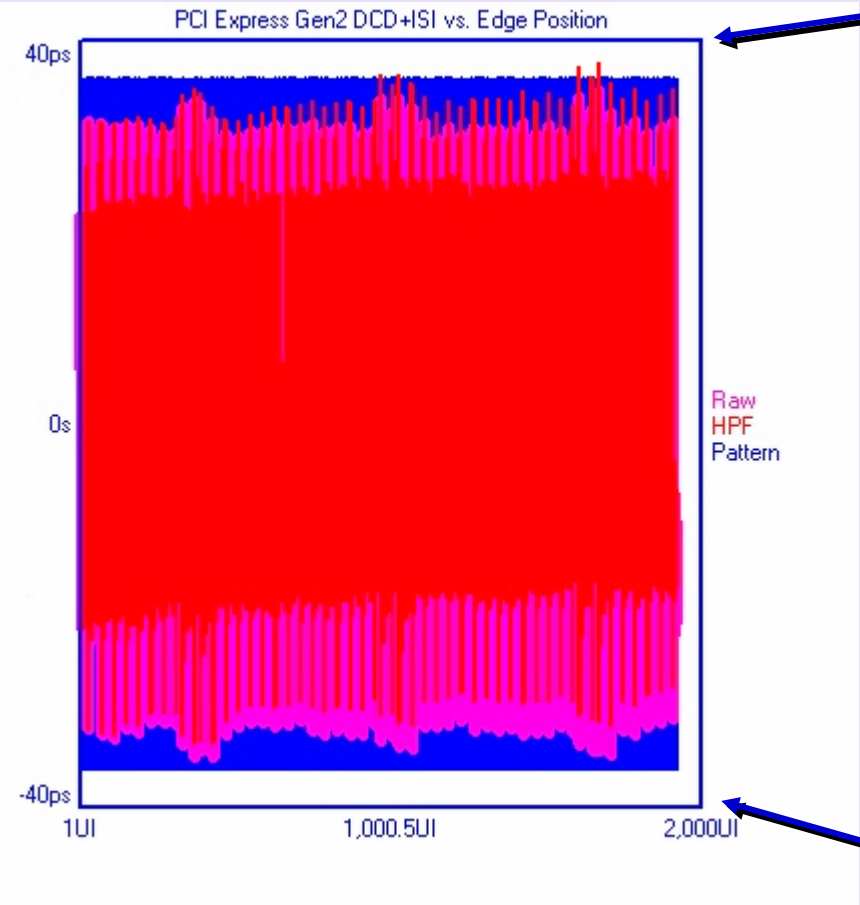
Rx Testing: DJ and TJ

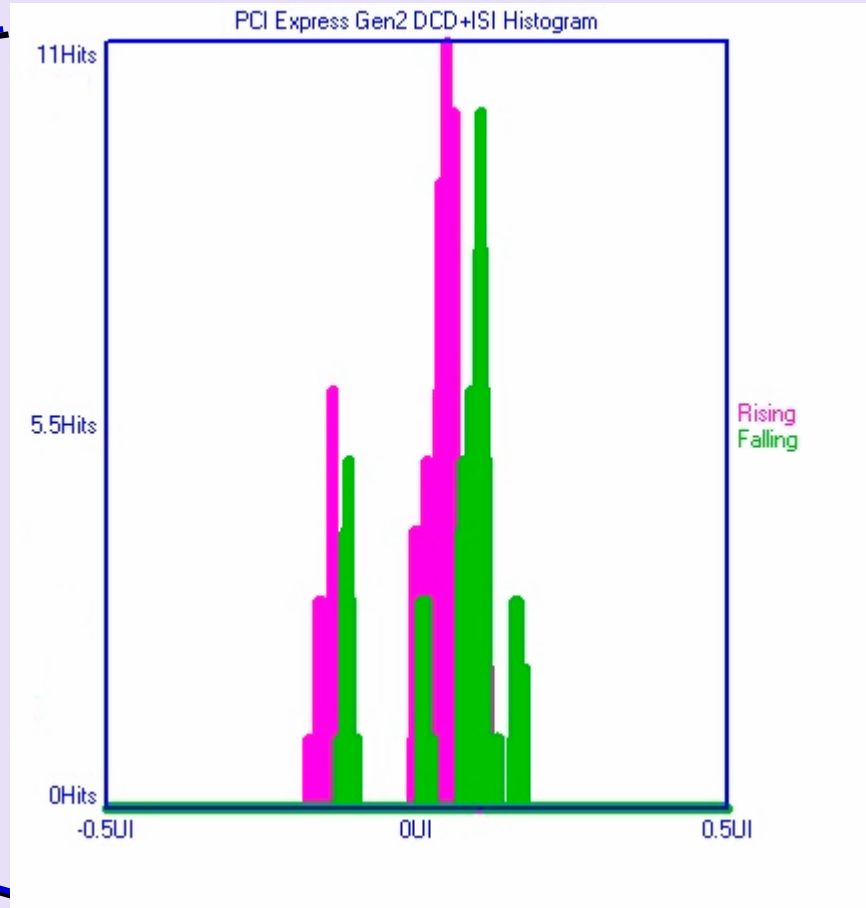


TIMING MEASUREMENTS

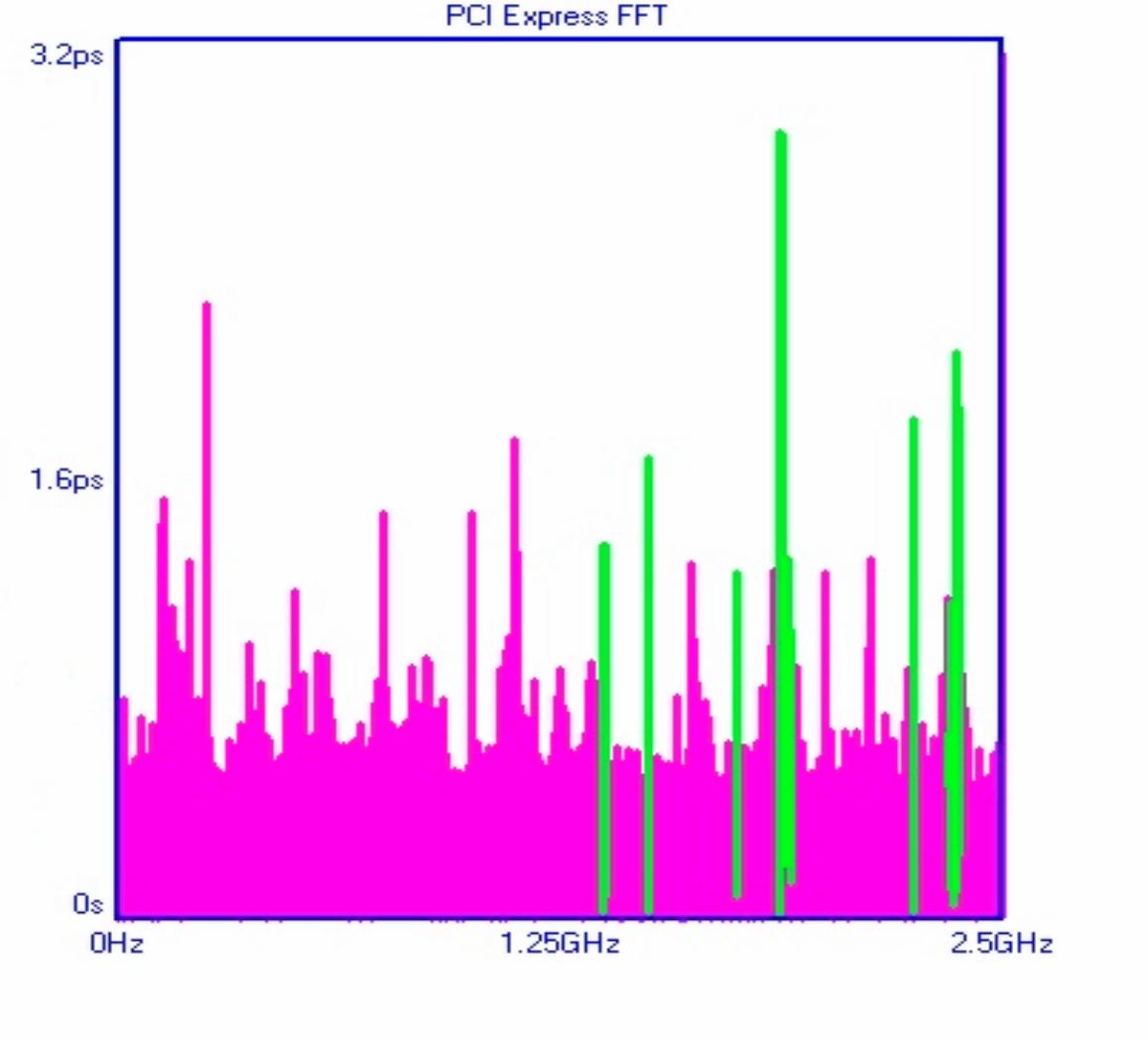
Quantity	Specification	Measured	Pass/Fail?
UI	199.94ps-200.06ps	200ps	PASS
TrxEye 10e-12	>0.40UI	0.478122UI	PASS
TrxDjDD	<0.44UI	0.284141UI	PASS
TrxRJ		0.016981UI	

Rx Testing: DDJ SPAN and Histogram

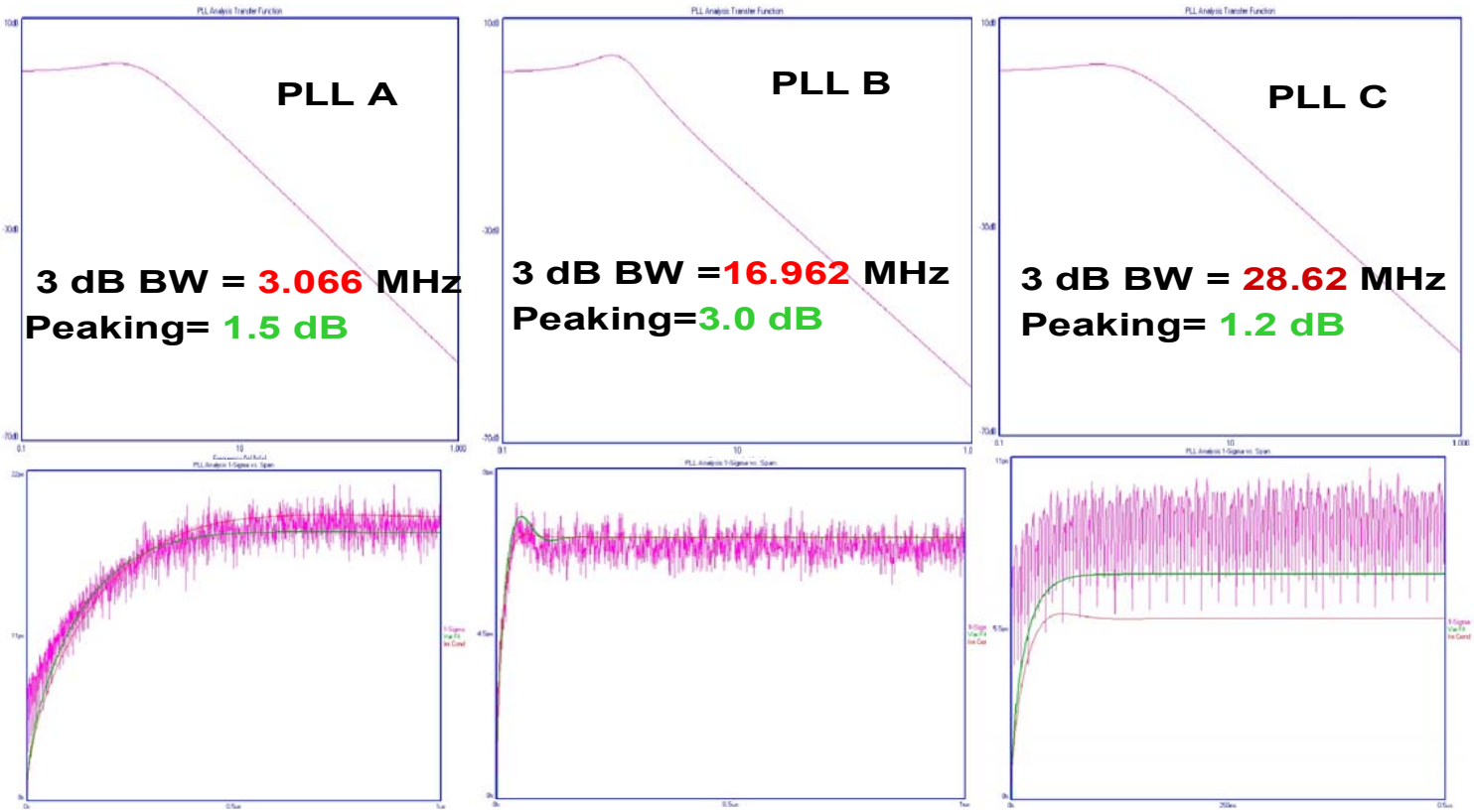




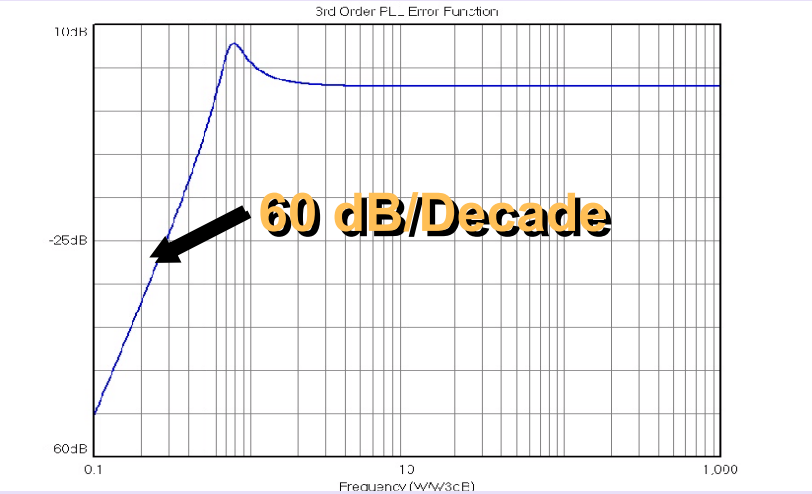
Rx Testing : PSD

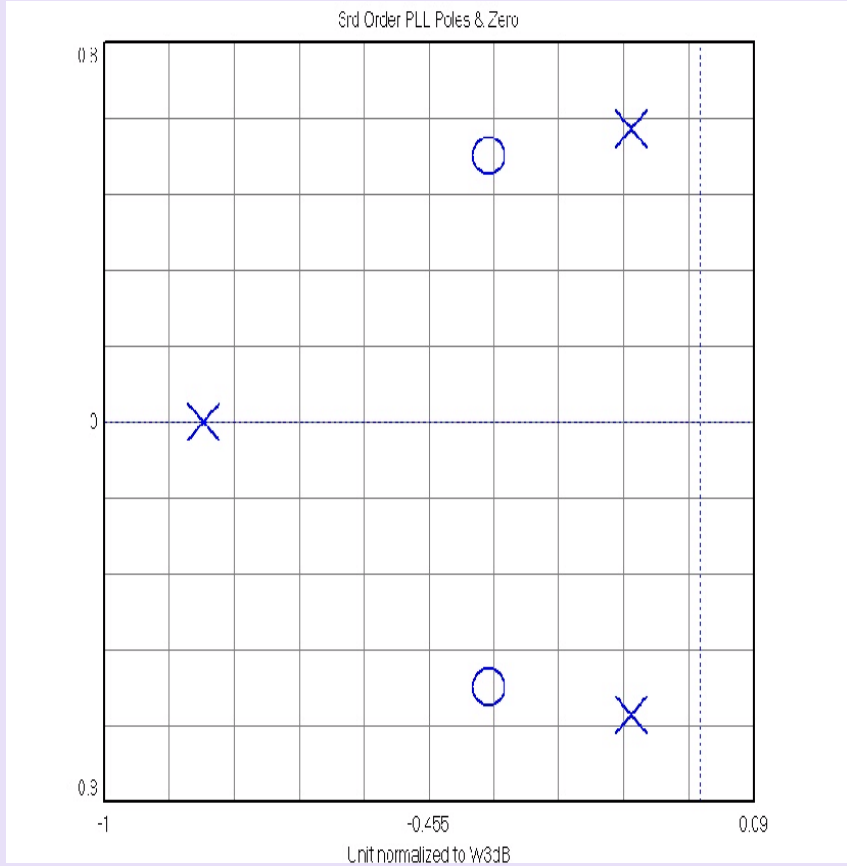


PLL Testing : 3 dB Frequency and Peaking

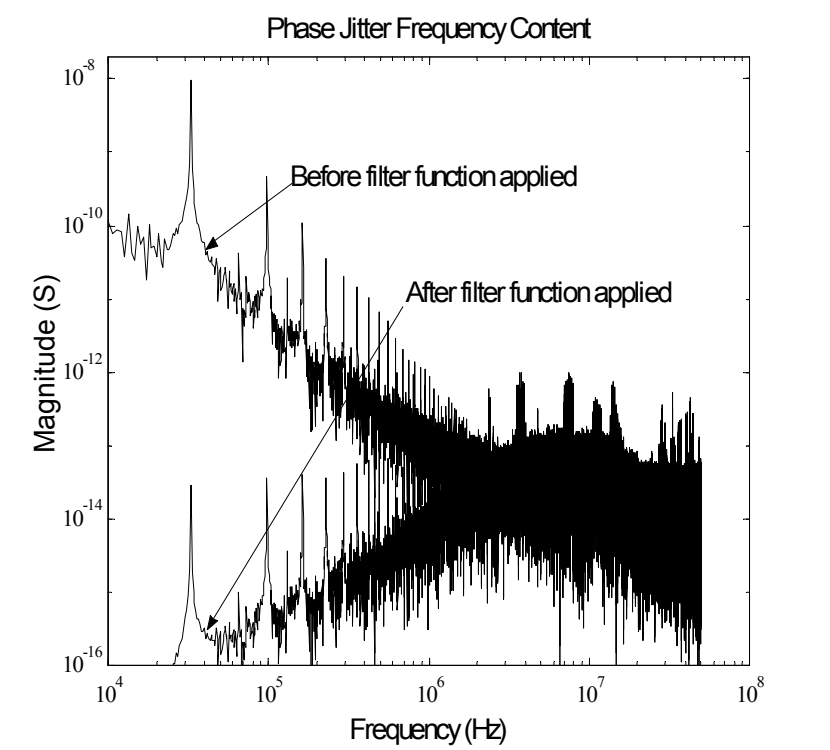


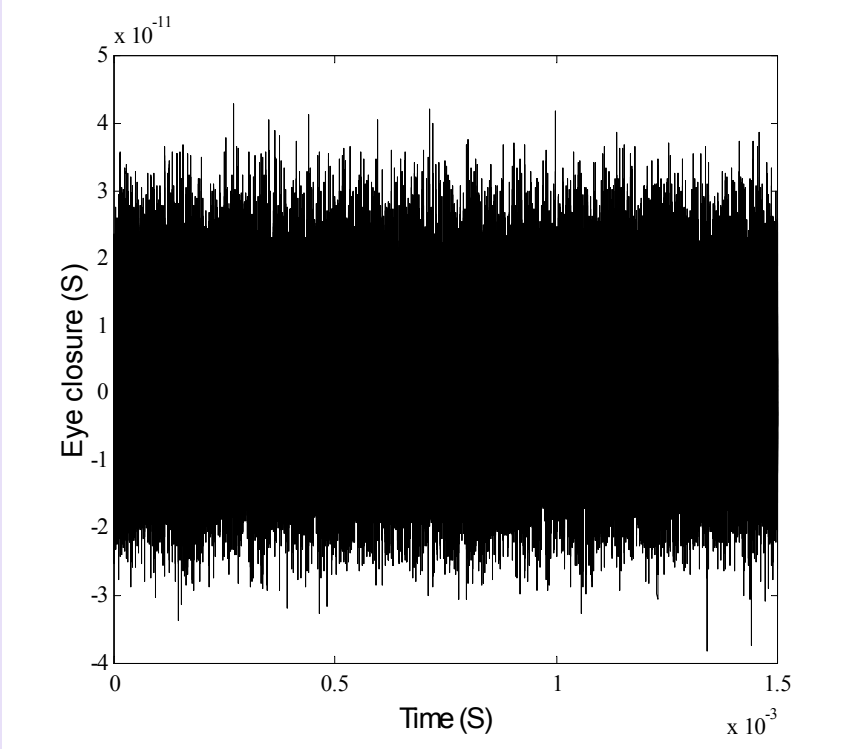
PLL Testing : A 3rd Order Case





Reference Clock Testing





RJ_rms = 8.31 ps > RJ_rms = 3.1 ps of specification

FAIL

V. Summary and Conclusion

- Signal integrity is composed of both Timing Jitter and Amplitude Noise
- Quantifying jitter and noise components is essential
- Understanding different jitter measure types is critical and phase jitter is used for PCI Express
- Transfer function is a must for testing serial links
- DJ/RJ/TJ testing are all critical and required for 5GT/sec
- PLL parameters are critical for PCI Express interoperability test
- Both compliance and diagnostic tests are needed in order to have a full test coverage

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CTO

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